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RANDOM LOGIC OXIDE SCREENING METHODS

Martin Marietta Space Systems

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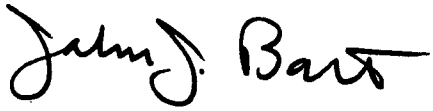
APPROVED: 

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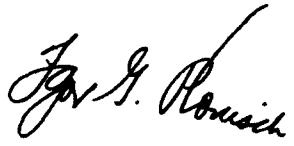
FOR THE COMMANDER: 

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13. ABSTRACT (Maximum 200 words)

This report covers the work performed on the Random Logic Oxide Screening Methods study in which techniques were investigated to improve oxide reliability screening methods in CMOS random logic devices. This effort included modeling of time dependent dielectric breakdown in state-of-the-art gate oxides, development of both internal and external screening techniques, and the performance of a screen and accelerated life test to verify predicted screening effects.

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EVALUATION

RANDOM LOGIC OXIDE SCREENING METHODS

The objective of this effort was to develop and demonstrate new methods for applying oxide reliability screen tests to random logic circuits. In memory devices, oxide fields are related to data stored and supply voltage. In random logic devices, oxide fields are related to circuit function and test pattern sequence. It is not hard to compose circuits and test sequences which exhibit node-to-node duty cycle differences of orders of magnitude. This results in uneven aging if straight functional test patterns are used during screening. For instance, screening an oxide with low stress duty cycle to a minimum effective age may exceed a maximum effective age for an oxide with a high stress duty cycle. This has been referred to as "...the duty cycle problem...", and it interferes with random logic screening. It is especially bothersome if there is persistent infant mortality, if there is an intermediate life failure distribution with an increasing hazard rate, or if the end of life failure distribution is very low and wide.

Supplier company responses to this problem are thought to range from doing nothing, to doing quite a lot. One view argues that we must emphasize process controls and other improvements to continuously push time zero defect densities down, hoping that early life failures will track down as well. Another view holds that even when burn-in yields get to be 99.99%, it will still be valuable to identify and reject that one device in ten thousand which contains a potential early life failure, and we should do what we can to make that happen during time-zero testing or burn-in, and not during field use.

We believe that both of the above views are correct. If the expected super reliable parts of the future do indeed have failure rates too low to measure, then we will be able to believe the numbers we use only if they are super built, super tested and super screened. Any other approach introduces risk that the supplier and the user must share. Until that risk really is vanishing, we believe that we should continue to improve testing and screening as well as design and manufacturing.

It is difficult to say whether the approaches to oxide screening in random logic parts described in this report have or have not been tried before. One was composing a special screening test vector, and the other was building in brute force screening modes. We conclude that it is very unlikely that either is a total solution. This study did not consider the effect of built in test techniques on screening, and that remains to be done.

Finally, the idea of in-process oxide screening has surfaced in several places. It would use a sacrificial metal mask at some point in the process flow to connect all gate oxides in parallel before they are wired to driving drains. Using this electrode and the substrate and well contacts, aging or non-aging screens can be performed. The cost of this method is added process steps and possibly some area penalty for modified contact and via layout. The benefit is 100% coverage, 100% even oxide screening, with little if any effect on performance. Implementation details and the test procedure are quite simple, and virtually all of the problems encountered with the methods studied in the present work are avoided. Unless new solutions to those problems are found, it would appear that in-process screening is the most promising method for screening to assure the quality of super reliable oxides.

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RADC/RBRP

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1. Introduction

1.1 General

The objective of this study is to determine and evaluate new methods of applying oxide reliability screen tests to CMOS random logic integrated circuits in order to reduce the incidence of in-field failures due to time dependent dielectric breakdown (TDDB). This effort is broken down into three major subtasks: oxide modeling, screening technique development, and test.

1. **Oxide Modeling:**
   The oxide modeling task consists of fabricating and testing some special structures in order to measure the characteristics of TDDB for a particular gate oxide.

2. **Screening Techniques:**
   The screening techniques task involves developing methods for improving oxide reliability screen tests. This task will include developing special internal circuitry to aid in screening as well as developing new techniques for improving screening tests via externally applied test vectors.

3. **Test:**
   The test task consists of designing, fabricating, and testing an oxide reliability test vehicle. This test vehicle will incorporate internal screening circuitry and will be subjected to the internal and external screening methods mentioned above. Finally a 4000 hour accelerated life test will be performed on the test vehicles to observe differences in failure rates between unscreened devices and those screened with the various screening methods developed.

1.2 Time Dependent Dielectric Breakdown

Current flows in a dielectric when a voltage field is applied across it. This current results from Fowler-Nordheim tunneling of electrons. These electrons are emitted from the cathode, travel through and interact with the oxide, and leave through the anode. Fowler-Nordheim current is described by the following expression (Ref 1 and 2):

$$j = AE^2 e^{-B/E}$$

where,

j = electron current density,
E = electric field (at the cathode), and
A,B are experimentally determined constants.

Common values for A and B are: A = 1.25E-6 A/V^2 and B = 233.5 MV/cm. Substituting values of electric field into this equation yields the current versus field relationship of figure 1. The shape of this curve resembles that of a forward biased diode with its inflection point at 6.7 MV/cm while using a current scale in the nanoamp range.

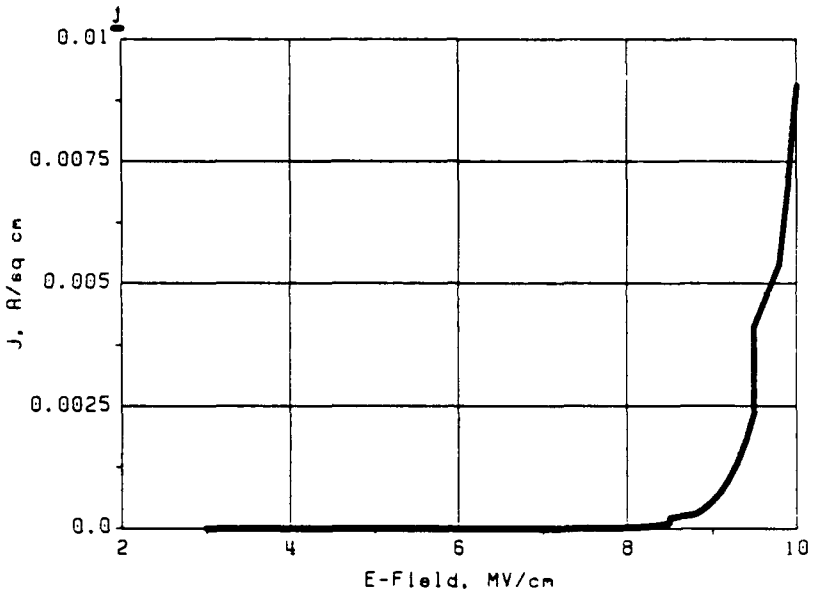


Figure 1 Injected Current Density as a Function of E-Field

Time-dependent dielectric breakdown is highly accelerated by an electric field as figure 1 indicates. The total current flow has been identified as the principal factor controlling dielectric breakdown. Because the current flow is important for predicting dielectric breakdown, the integral of the current over time is a key element in TDDB screen tests.

If the current in the dielectric strictly followed the Fowler-Nordheim current/voltage relationship, the acceleration factor related to an electric field change would be easily understood. The log of current would be proportional to the inverse of the electric field. Unfortunately there are a number of other factors which dominate. The principal factor is the charge developed within an oxide during current injection.

When a constant voltage is placed across an oxide, a current flows through the oxide that follows a transient controlled by local field effects. Electron injection from the silicon into the oxide produces a buildup of positive charge near the Si-SiO_2 interface (Ref 3, 4, and 5). This creates fast interface states at the Si-SiO_2 interface and produces electron traps in the bulk of the oxide. Electrons are injected into the oxide and gain kinetic energy as they travel toward the anode. The energy they gain however, is not very high because it is dissipated by multiple interactions in the dielectric. The total energy gain in a 10 MV/cm field will be only a few electron volts which is not enough to create electron-hole pairs. The primary function then of the field is just the injection of the electrons into the oxide. These electrons will have the potential energy related to being in the oxide-conduction band. This energy is lost when an electron is trapped or when it leaves the dielectric at one of the electrodes. When they lose this energy, they cause damage which is permanent and cumulative.

The positive charge created near the $Si-SiO_2$ interface is referred to as anomalous positive charge because it is produced by the injection of electrons. The effect of this charge is to enhance the current injection when an electric field is first applied.

The fast interface states that are created are filled with electrons and these retard the electron injection. The production of these states saturates rapidly and the total number produced largely depends upon the oxide processing.

The electron traps that are produced in the oxide are partially filled with electrons and these also retard the electron injection. Electron traps are continually being generated during the current injection. The probability of electron trap generation varies with electric field. It is approximately 0.01 cm^{-1} at 4 MV/cm and increases to 0.1 cm^{-1} at 9 MV/cm. The occupation, and therefore the effect on current flow, is also a function of electric field. With electric field, electrons are detrapped from these sites so that the percent of trap occupancy is lower at high fields and higher at low fields. A field dependent occupation of traps and a field dependent generation of traps produces a slowly increasing net negative charge in the oxide. As a result the injected current slowly tapers off with time.

Electron traps have an additional effect besides the modification of the current transient. It has been proposed that when a certain density of electron traps is reached, dielectric breakdown occurs. This value has been reported as about 10^{20} cm^{-3}. This will provide a spacing of traps between which electrons can tunnel.

The above discussion was related to the decrease in time to failure with increasing fields resulting from additional current flow. Temperature has also been shown to accelerate dielectric breakdown. The most commonly reported value for the temperature effect is an activation energy of 0.3 eV. This is relatively weak with respect to the acceleration related to electric field.

1.3 Simplified TDDB Model

This program is using a simplistic model for TDDB when compared to that presented above. We are assuming that for the purposes of developing screening techniques the injection current through the gate oxide is constant with time and follows an approximate form of the Fowler-Nordheim tunneling equations:

$$j \propto e^{-B/E}$$

Let us now derive some equations which will be needed when dealing with the statistics of oxide defects and TDDB. Let us first define the density of defects leading to breakdown at or below a certain applied E-field to be D(E). We will note now that the defect density D can also be defined in terms of injected charge density or as a function of time (for a fixed field). From now on we will simple refer to D instead of the explicit form D(E,Q,t).

For an oxide of area A we define μ to be the number of defects leading to breakdown:

$$\mu = D \cdot A$$

We assume that when the defects are distributed at random over the surface the probability that x defects failing at or below an E-field 'E' is given by the Poisson distribution:

$$f(x,\mu) = \frac{\mu^x}{x!} e^{-\mu}$$

The probability that $x \geq 1$ is obtained by summing this over the interval $1 \geq x \geq \infty$.

$$F(\mu) = \sum f(x,\mu)$$

The function $F(\mu)$ is interpreted as the probability of having a defective oxide which will fail at or below some applied E-field E. The summation from 1 to infinity however would be somewhat tedious to perform. An alternate expression is possible however. We can express the probability of having x = 0, i.e. the probability of having no defects present which fail at or below E.

$$F_0(\mu) = f(x,\mu)\,|_{x=0} = e^{-\mu}$$

Also, by definition, the sum of F and F_0 must equal 1 since they are the probability of having x greater than equal to 1, and x equal to 1, respectively.

$$F(\mu) + F_0(\mu) = 1$$

Thus, by substituting our expression for $F_0(\mu)$ into this last equation we have:

$$F(\mu) = 1 - e^{-\mu}$$

We are now interested in deriving an expression for the defect density D. We may solve this last equation for μ and then substitute in our initial equation $\mu = D \cdot A$:

$$\mu = D \cdot A = -\ln(1-F(\mu))$$

$$D = (1/A)(-\ln(1-F(\mu)))$$

Now let us define a normalized defect density D' by multiplying by some reference unit of area A' (we do this to allow the following manipulations where D must be a dimensionless quantity). We will use this final formula extensively to extract the defect density from our oxide characterization data.

$$D' = D \cdot A' = (A'/A)(-\ln(1-F(\mu)))$$

$$\ln D' = \ln(-\ln(1-F(\mu))) - \ln(A/A')$$

1.4 References

1. D. Schroder and R. Thomas: Experimental Confirmation of the Fowler-Nordheim Law for Large-Area Field Emitter Arrays. Appl Phys Lett. Vol 23, No. 1, July 1973.

2. Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky: Measurement of Fowler-Nordheim Tunneling Currents in MOS Structures Under Charge Trapping Conditions. SSE, 28, No. 7, 1985.

3. D. Wolters and J. Van Der Schoot: Dielectric Breakdown in MOS Devices, Part I: Defect-Related and Intrinsic Breakdown, Part II: Conditions for the Intrinsic Breakdown, Part III: The Damage Leading to Breakdown. Philips Journal of Research, Vol 40, No. 3, 1985

4. Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky: Trap Generation and Occupation Dynamics in SiO_2 Under Charge Injection Stress. Journal of Applied Physics, Vol 60, No 6, September 1986.

5. H. Boesch and J. McGarriety: An Electrical Technique to Measure the Radiation Susceptibility of MOS Gate Insulators. IEEE Transactions on Nuclear Sciences, Vol. NS-26, No. 6, December 1979.

6. I.C. Chen, et. al., "A Quantitative Physical Model for Time Dependent Breakdown in SiO2", 23rd Annual Proc., IEEE International Reliability Physics Symposium, 1985, pp. 24-31.

7. A. Berman, "Time Zero Dielectric Reliability Test by a Ramp Method", 19th Annual Proc., IEEE International Reliability Physics Symposium, 1981, pp. 204-209.

2. Oxide Modeling

In order to predict the failure rates seen during the accelerated life testing of the test vehicles, it is necessary to model the effects of TDDB on the gate oxide. A computer program known as the Oxide Stress Analyzer (OSA) was developed to perform this modeling.

The OSA has two basic uses: modeling the effects of TDDB on a particular gate oxide, and analyzing the effectiveness of different test vector sets in evenly stressing a design. The second usage of the OSA will be covered in sections 3 and 4. Here we will discuss its use in modeling TDDB.

The OSA is designed to take raw data collected while overstressing test capacitors and analyze it in order to predict the effects of stress on the gate oxide in a real design. It is designed to accept raw capacitor breakdown data in three different forms: time to breakdown, E-field at breakdown, or total injected charge at breakdown. It can then analyze this raw data in order to provide various plots of breakdown data with respect to time, E-field, and injected charge density. In addition, the OSA can perform linear regression analyses on this data in order to provide a mathematical model of breakdown. Thus, the operation of the OSA may be broken down into three functional blocks: data collection, data reduction and plotting, and data analysis. For details of the actual commands used by the OSA, please refer to the OSA help file listed in appendix A.

2.1 Data Collection

Data collection is actually performed in four steps. The first step is to read in raw data taken from the test setup. More information on the test setup may be found in section 2.5. This data consists of stored waveforms from the digital storage oscilloscope along with some setup information.

Figure 2 shows an example of the raw input and output waveforms taken by the storage oscilloscope. This raw data is parsed by a program called the Data Pre-Processor (DPP).

The DPP extracts from this raw data the time, E-field, and injected charge necessary to break down each capacitor. The DPP is configurable so that non-ideal behavior of the test fixture (such as offset voltage) may be accounted for. The DPP also allows the user to define exactly what condition should be considered to be "breakdown." For instance, the output waveform is actually a measure of the current being injected through the test capacitor to ground. The bigger the capacitor, the bigger this injected current. Thus the DPP allows the user to specify different breakdown levels for the different size capacitors so that the same current density is used to determine the breakdown point. Finally the DPP includes data smoothing algorithms which are used to reduce some of the electrical noise which is apparent in the data.

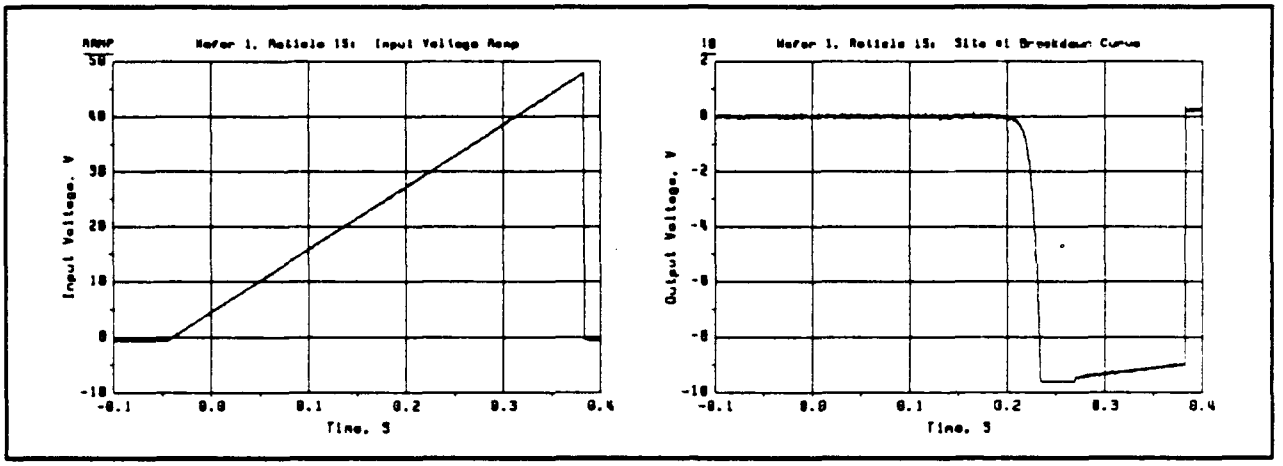


Figure 2 Raw Input and Output Waveforms

The final data produced by the DPP consists of identification information for each capacitor as well as the time and injected charge required to break them down. Following is an example of the output of the DPP. There is first a short header which gives some general information. Following this are four lines which identify which capacitors are contained in the file as well as the test type (ramp or fixed voltage stress), test temperature, and the date the test was performed. Finally for each capacitor the time to breakdown and the total injected charge at breakdown is recorded along with a code (A, B, or C) which signifies the capacitor's size.

```
#
# Analysis of data file "w1r38.sb".
#
# Time & date of analysis:  14:19:24, JAN 31, 1989.
#
# Time & date of data collection:  15:19:42, 24-OCT-88.
#
# Smoothing:  On, Granularity = 10 data points.
#
# Exception Processing:  Off.
#
# Ramp window:  0.11, 0.33 (seconds).
#
# Bias window:  -0.125, 0.125 (volts).
#

ID:     SUBS W1 R38
TTYPE:  RAMP 113.365
TTEMP:  27.0
DATE:   24-OCT-88
```

```
CAP:      1 B
BTIME:    0.242
BCHARGE: 3.71987e-05

CAP:      2 A
BTIME:    0.2435
BCHARGE: 9.14153e-06

CAP:      3 B
BTIME:    0.242
BCHARGE: 7.62208e-05

CAP:      4 A
BTIME:    0.246
BCHARGE: 7.77687e-05

CAP:      5 C
BTIME:    0.2425
BCHARGE: 0.000111693

CAP:      6 C
BTIME:    0.2415
BCHARGE: 5.24763e-05

CAP:      7 B
BTIME:    0.2425
BCHARGE: 9.59599e-05

CAP:      8 A
BTIME:    0.245
BCHARCE: 8.43794e-05

CAP:      9 B
BTIME:    0.242
BCHARGE: 5.39811e-05

CAP:      10 A
BTIME:    0.2405
BCHARGE: 0.000114901

CAP:      11 C
BTIME:    0.2405
BCHARGE: 2.4692e-05

CAP:      12 C
BTIME:    0.2405
BCHARGE: 6.90209e-05
```

This data is then parsed by the OSA database building routines. These routines add the capacitor data to a database which allows for easy access by other OSA modules. In addition, if the test type was ramp, the OSA calculates the E-field at breakdown (based on the time to breakdown and the stress voltage ramp rate) and adds this information to the database.

The final step in data collection involves extraction of a portion of the database for further analysis. This is necessary in order to compare results for capacitors of different types and sizes, data taken from different wafers, or data taken using different test types. For instance, if the user desires to analyze data from only solid substrate capacitors taken from one particular wafer using a ramp voltage test the OSA has the capability of extracting only this data from the database and ignoring the rest.

2.2 Data Reduction and Plotting

Once a particular subset of data has been extracted from the OSA database, several things may be plotted. These are:

1. Instantaneous percent failures (f),
2. Raw cumulative percent failures (F),
3. Cumulative percent failures (CPF), and
4. Defect density (DD).

These quantities may be plotted as a function of any of the three indices:

1. (log) Time,
2. E-field, or
3. (log) Injected charge density.

The user may choose any level of resolution or granularity for the plots. Higher resolution (lower granularity) data reduction and plots require more CPU time but are more accurate.

2.3 Data Analysis

The primary data analysis which may be performed by the OSA is a linear regression analysis of any plot data. To do this, the user selects a particular x-axis range of data which is then analyzed to find the equation of the straight line which best fits the y-axis data. This information may be used in several ways.

First this equation enables one to express the cumulative failures as well as the instantaneous failure rate of a given oxide area in analytic form. This allows the user to predict the instantaneous failure rate for this particular oxide area and stress. This is illustrated in figure 3. Performing a linear regression on this set of data in the range ($0.5 < x < 7.5$) results in an

expression for cumulative percent failure of:

$$CPF = (0.03\ cm/MV)x + (-3.37)$$

From this, expressions may be derived for raw cumulative percent failure (F) and instantaneous failure rate (f). First let us define m as the slope and b as the y intercept of the CPF equation obtained by performing a linear regression analysis on the CPF data. Thus:

$$CPF(\ln(-\ln(1-F))) = mx+b$$

$$F = 1 - e^{-[e^{(mx+b)}]}, \text{ and if } x=\ln(t),$$

$$F = 1 - e^{-t^m e^b}, \text{ and}$$

$$f\ (\ dF/dt\ ) = (t^m e^b e^{-t^m e^b})(e^b m t^{(m-1)}).$$

Figure 4 displays the instantaneous failure rate calculated with the previous formula for our example cumulative percent failure plot. Included for reference on the same chart is the CPF curve used in the calculations. It is important to note that in this example the instantaneous failure rate is a monotonically decreasing function. This is always the case for a low defect oxide because the slope of the CPF curve (m) is always small. Theoretically it is thus possible to develop a screen for TDDB. For example, if a failure rate of 0.001% is desired, the screen should be a ramp to 4 MV/cm which is equal to 12V for a 300 angstrom oxide. The question remains however as to whether the voltages and times involved in such a screen are practical.

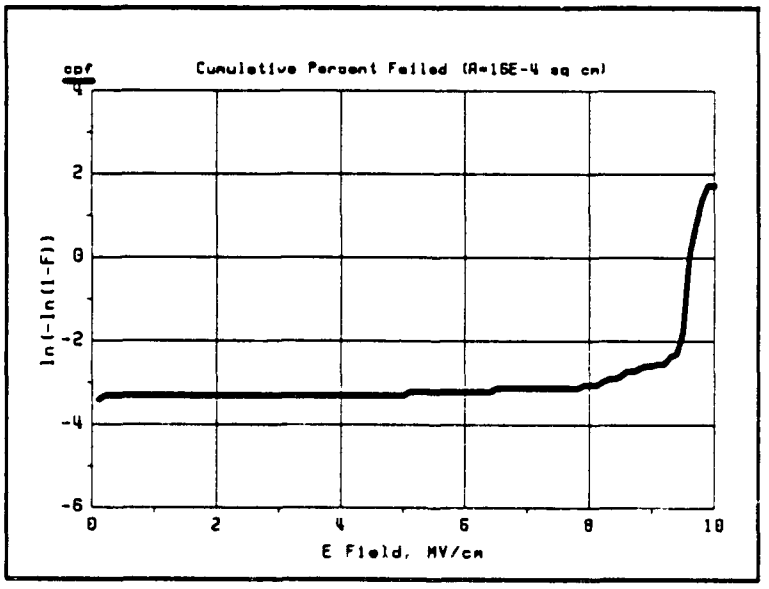


Figure 3 Example Cumulative Percent Failure Plot

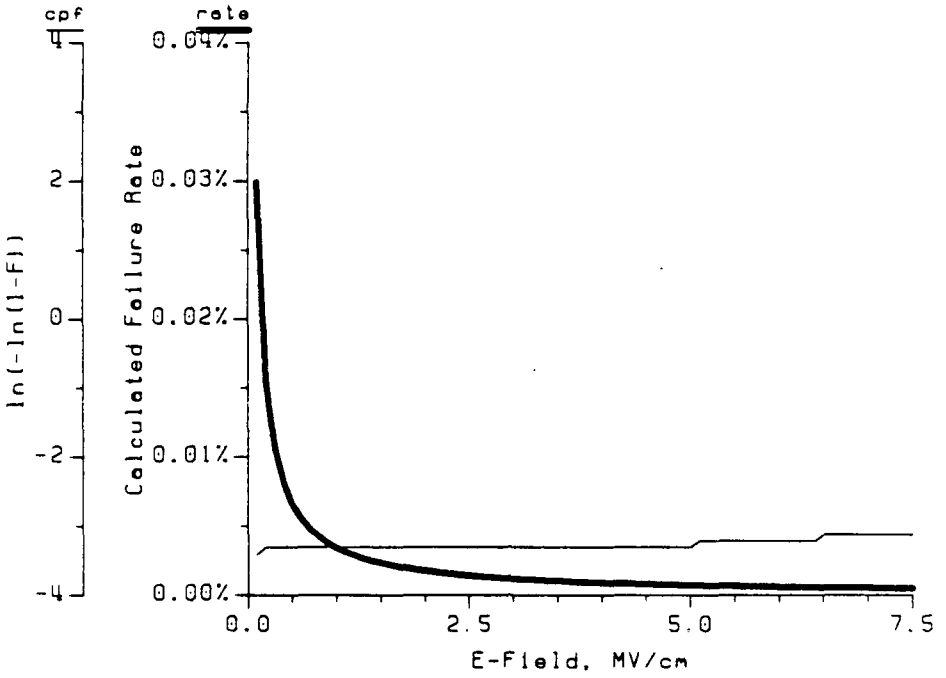


Figure 4 Example Instantaneous Failure Rate Curve

Performing a linear regression analysis on the data allows more powerful expressions to be derived as well. For instance figure 5 shows three separate curves of cumulative percent failure. Each of these curves represents data taken from different size capacitors. When a linear regression is performed on the three curves (over the range 0.1 to 7.5 MV/cm) the following equations are obtained for cumulative percent failure:

$$\text{CPFA (area = 4.0E-4 cm}^2\text{)} = (0.03\ \text{cm/MV})x + (-5.7),$$

$$\text{CPFB (area = 8.0E-4 cm}^2\text{)} = (0.03\ \text{cm/MV})x + (-4.4), \text{ and}$$

$$\text{CPFC (area = 1.6E-3 cm}^2\text{)} = (0.04\ \text{cm/MV})x + (-3.4).$$

If now the change in the y-intercept of the three curves is noted, an expression can be derived for the oxide area acceleration factor. As was discussed in section 1.2 the acceleration factor is expected to be ln(A) where A represents the area of the oxide divided by some unit measure of area. Figure 6 shows the three y-intercepts plotted as a function of A while figure 7 shows these y-intercepts plotted as a function of ln(A). Notice that figure 7 yields a straight line with a slope of +1 which confirms that the oxide area acceleration factor is indeed ln(A).

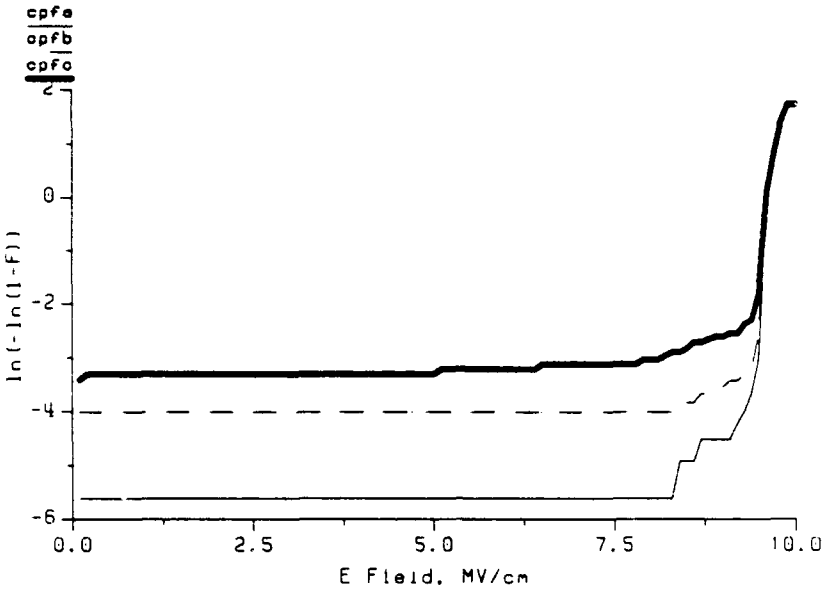


Figure 5 Example Plot for Calculating Acceleration Factors

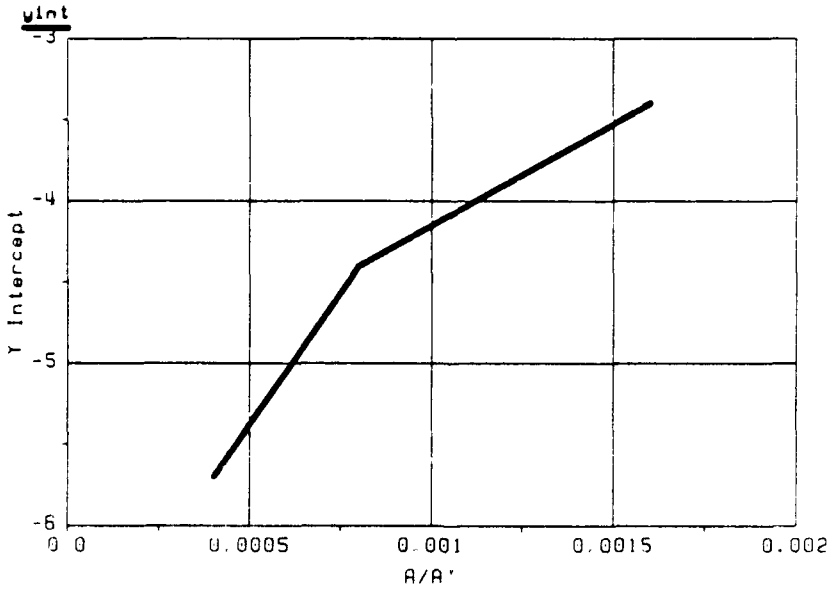


Figure 6 Y-Intercepts as a Function of A

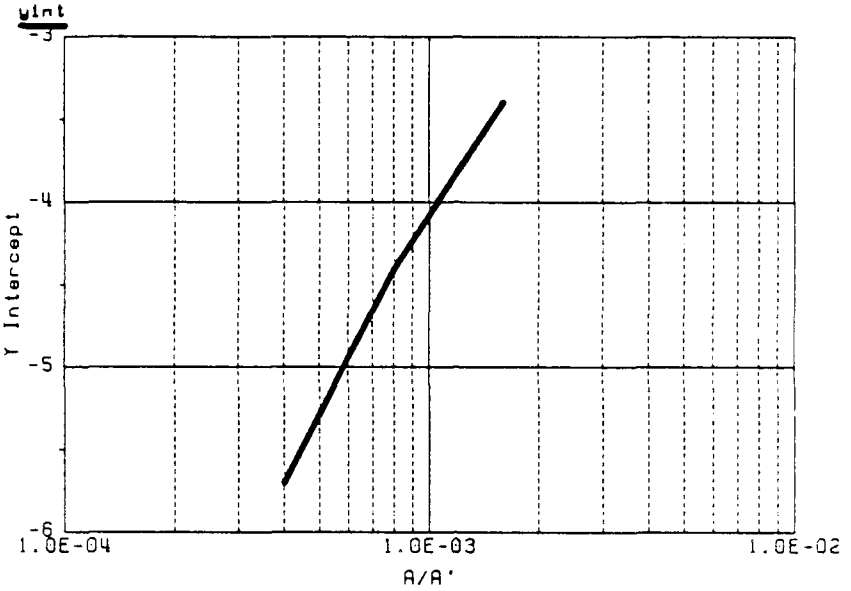


Figure 7 Y-Intercepts as a Function of ln(A)

2.4 Oxide Characterization Test Structures

In order to characterize the gate oxide it is necessary to fabricate special test structures. The ideal candidates for this purpose are very large capacitors with the gate oxide forming the dielectric. The reason for this is twofold. First capacitors are quite simple to stress, requiring only two probe contacts. More important however is that a capacitor is the most efficient structure for getting a maximum of gate oxide area in a minimum of physical space. It is necessary to have this high gate oxide area since state of the art MOS processes have very high quality gate oxides with low defect densities. Four separate test structures were designed and fabricated in order to characterize the gate oxide. The four types were:

1. **Solid Substrate Capacitors (SUBS):** These capacitors consist of large, solid gate oxide capacitors. They are formed by placing a plate of gate polysilicon completely covering a very large active area region. This creates a capacitor with the gate polysilicon forming one plate, the gate oxide forming the dielectric, and the lightly n-type substrate forming the other plate. The solid substrate capacitors were fabricated in three different sizes: 4.0E-4 cm^2, 8.0E-4 cm^2, and 1.6E-3 cm^2. These different sizes were created in order to study the effect of total oxide area on failure rates. The graphical layout of the smallest size solid substrate capacitor is shown in figure 8.

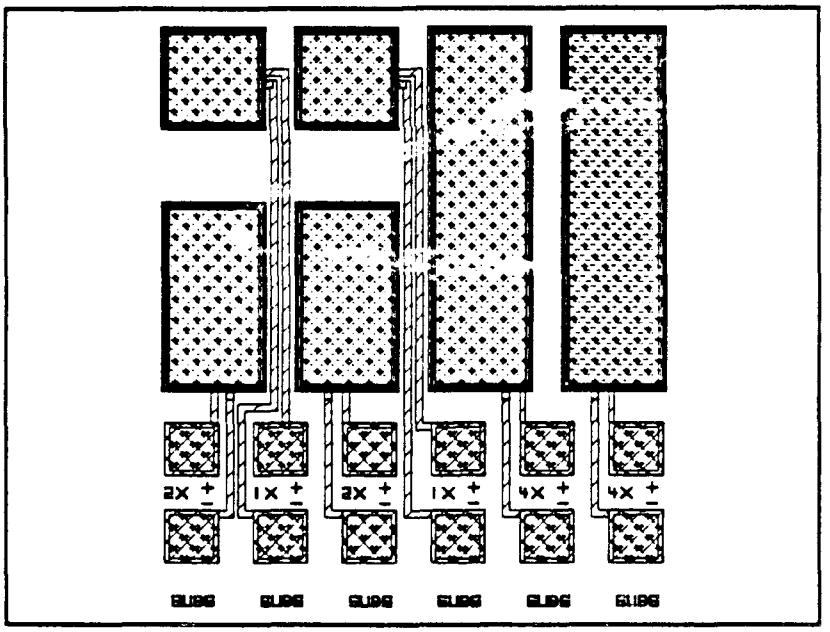


Figure 8 Solid Substrate Capacitor Layout

2. **Solid P-Well Capacitors (PWELL):** These capacitors are almost identical to the solid substrate capacitors discussed above. They are formed in exactly the same manner and were fabricated in exactly the same sizes as the solid substrate capacitors. The only difference is that the solid p-well capacitors were formed in the p-well rather than on the n-type substrate. Thus while the gate polysilicon still forms one plate, and

the gate oxide forms the dielectric, the second plate is in this case formed by the p-type well rather than the n-type substrate. These capacitors were designed and fabricated in order to see if there was any difference in the oxide characteristics between the n-channel and p-channel transistors used in CMOS. The layout of the smallest size solid p-well capacitor is shown in figure 9.

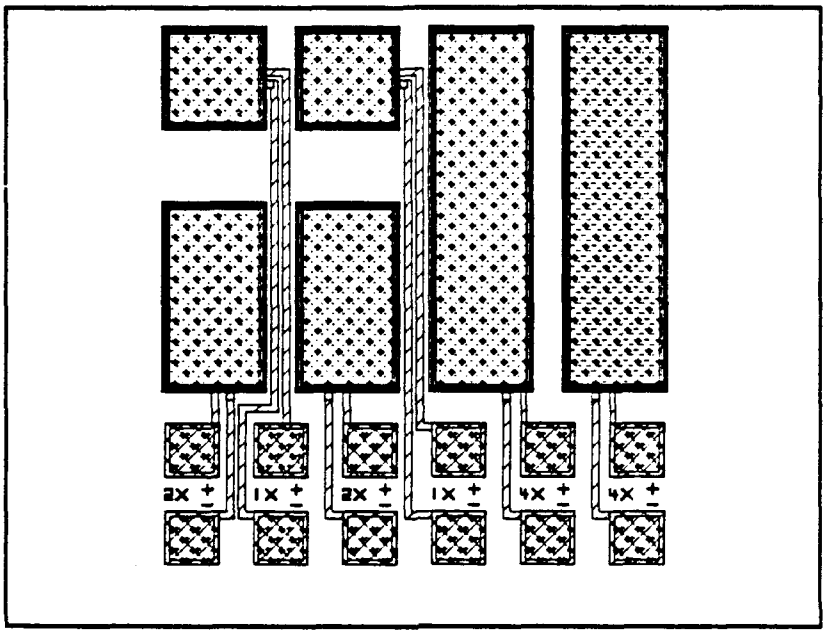


Figure 9 Solid P-Well Capacitor Layout

3. **Multi-Stripe N-Channel Transistors (NCH):** These test structures were created in order to better determine how to model the gate oxide in an actual transistor. They are very large multi-stripe n-channel transistors with a total gate oxide area of 4.0E-4 cm^2 (the same area as the smallest solid capacitors.) The layout of one of these transistors is shown in figure 10. The reason that the gate oxide area of a transistor is more difficult to model than that of a capacitor is illustrated in figure 11. The gate oxide is actually divided into three regions: the main gate to channel region (A), gate to source overlap region (B), and a gate to drain overlap region (C). While in normal operation these three regions receive very different stress. For instance in an inverter, the gate to channel region as well as the gate to source overlap region are stressed only when the input voltage is at the opposite logic level compared to the power supply voltage tied to the source. However, the gate to drain overlap region is always stressed since the input and output of the inverter (the gate and drain of each transistor) are always in opposite logic states. Another complicating factor in modeling a transistor's gate oxide is that the periphery of the gate may have different breakdown characteristics than that of the bulk of the gate. This effect was not dealt with in the structures tested in this project.

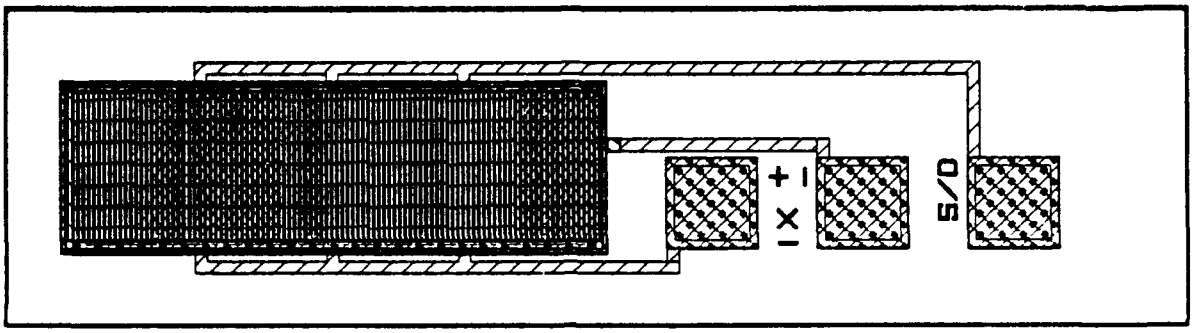


Figure 10 Multi-Stripe N-Channel Transistor Layout

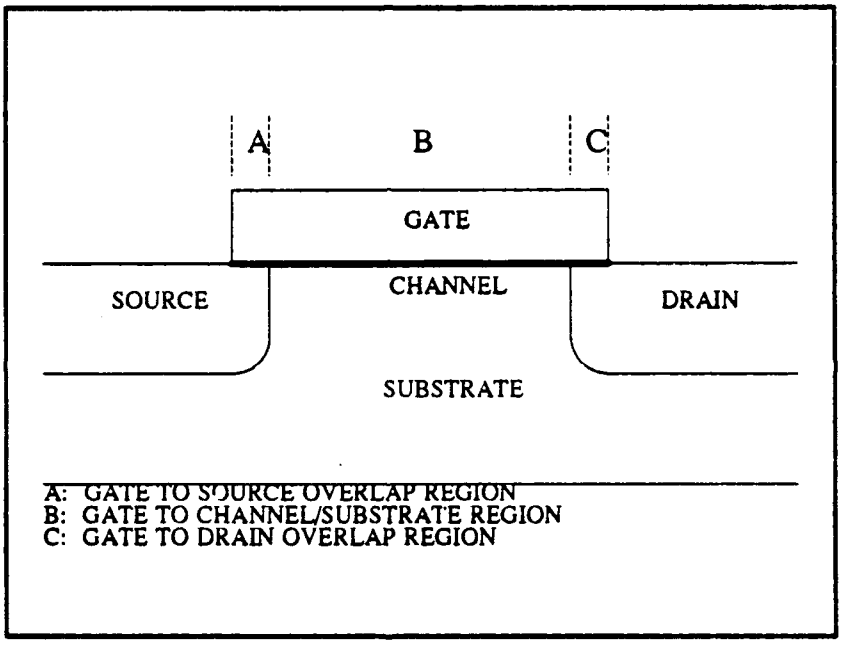


Figure 11 Transistor Gate Oxide Regions

The large multi-stripe n-channel transistor test structures are intended to provide information on exactly what proportion of the total gate oxide area belong to the three different regions. This information can be extracted by stressing the gate to channel region while not stressing the overlap regions. The failure rate information obtained from this may be compared to that obtained while stressing all three regions simultaneously. The difference in the failure rates for these two cases may be attributed to the "area effect" and thus the effective areas of each region may be calculated. Stressing of only the gate to substrate region may be accomplished by tying the gate, source, and drain of the transistor together and forcing all three nodes high with respect to the p-well. The stress applied in this case however must be well controlled to ensure that the parasitic diodes due to the source/drain to p-well junction do not suffer from reverse breakdown.

4. **Multi-Stripe P-Channel Transistors (PCH):** The p-channel multi-stripe transistors are identical in construction and size to the n-channel multi-stripe transistors except that the p-channel transistors are constructed on top of the n-type substrate as opposed to n-channel transistors formed in the p-well. They serve the same purpose as the n-channel transistor test structures but are needed since the lateral diffusion of the p+ source/drain implant in these transistors is different than the lateral diffusion of the n+ source/drain implant of the n-channel transistors. This results in different effective gate lengths and thus different proportions for the three gate oxide regions. The layout of one of these transistors is shown in figure 12.

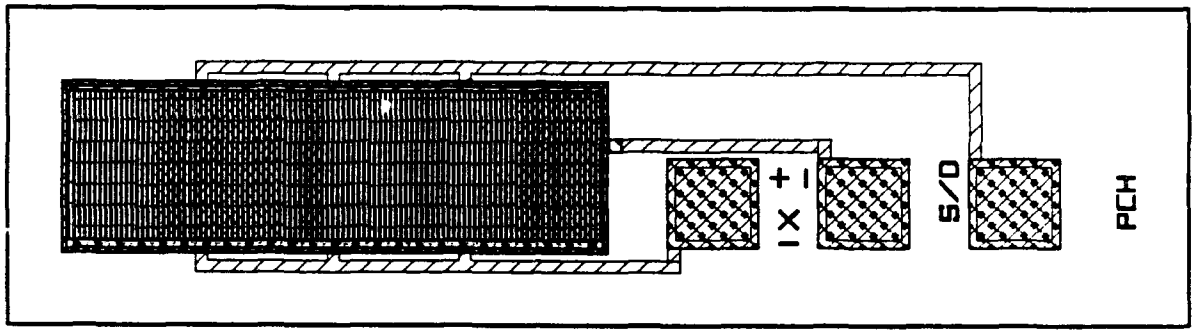


Figure 12 Multi_Stripe P-Channel Transistor Layout

These four test structure types were fabricated in a 2 micron double level metal CMOS process featuring 300 angstrom gate oxide thickness. Figure 13 is an optical microscope photograph of the resulting die area.

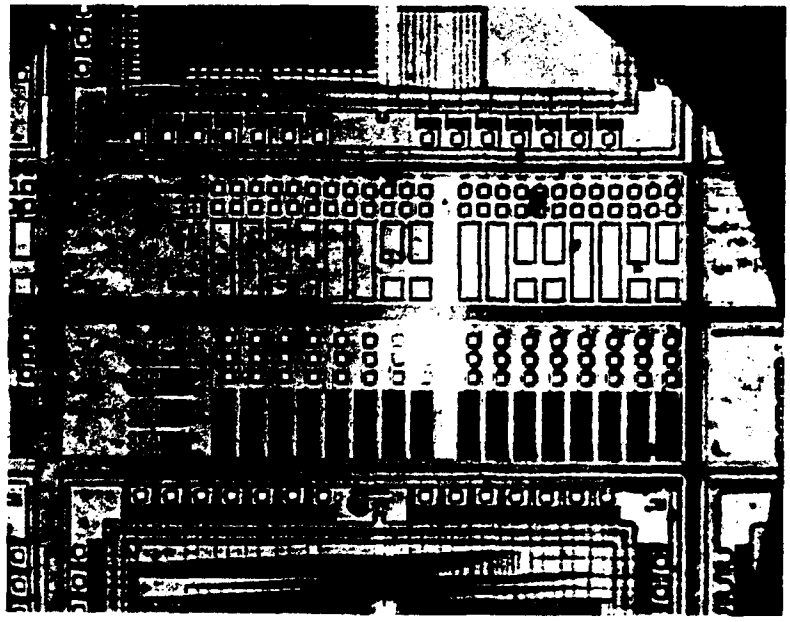


Figure 13 Oxide Characterization Structures Die Photograph

2.5 Oxide Testing Environment

The physical hardware used for stressing the test structures consisted of several instruments controlled using an IBM compatible personal computer through an IEEE-488 bus. This is illustrated in figure 14. The wafer probing was performed using a semi-automatic probe station equipped with micro-coaxial probes, the stress voltage was provided using a programmable power supply, and the data was acquired using a digital storage oscilloscope.

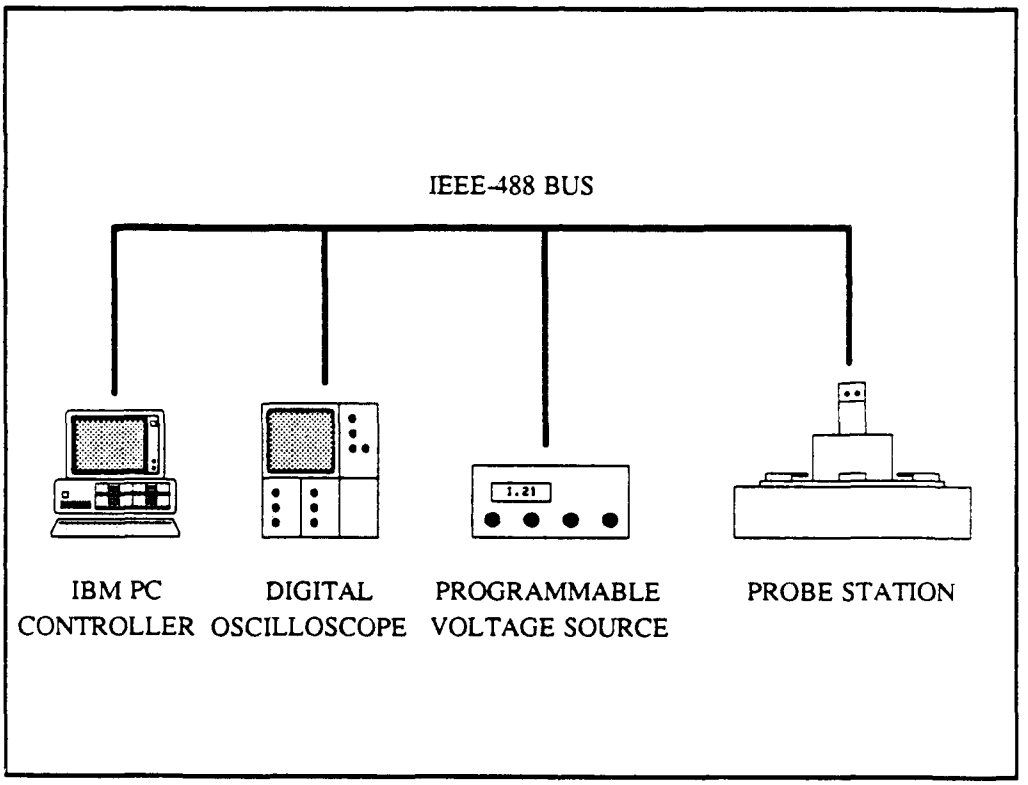


Figure 14 Oxide Testing Environment Hardware Setup

The basic theory of operation of this setup is that upon computer command the programmable power supply provides a controlled stress voltage directly to the device under test. As this is occurring, a special test fixture converts the current injected through the gate oxide into a voltage signal. The digital storage oscilloscope then captures both the stress input and breakdown waveforms for later analysis. The data from the oscilloscope is then stored in a file on the PC and finally transferred to an Apollo workstation to perform the analysis.

The special test fixture is quite simple in concept and is shown in figure 15. The inverting input of the operational amplifier is connected to the negative side of the device under test through a micro-coaxial probe. The non-inverting side of the operational amplifier is connected to ground and thus provides ground to the DUT through the opamp virtual ground (provided the slew rate limit and maximum output current of the opamp are never exceeded.) The feedback network is a simple resistor network and sets the trans-resistance of the circuit.

A single feedback resistor was not used since unreasonably high resistor values would be required to achieve high gain. The multiple resistor network allows for a high effective feedback resistance without resorting to high individual resistor values. The effective trans-resistance of the circuit is given by the following formula:

$$TR = R_f = (R_1R_2 + R_2R_3 + R_1R_3) / R_2.$$

Due to noise from the microscope probe station controller which was not successfully filtered out, a relatively low transresistance of 12,000 was selected.

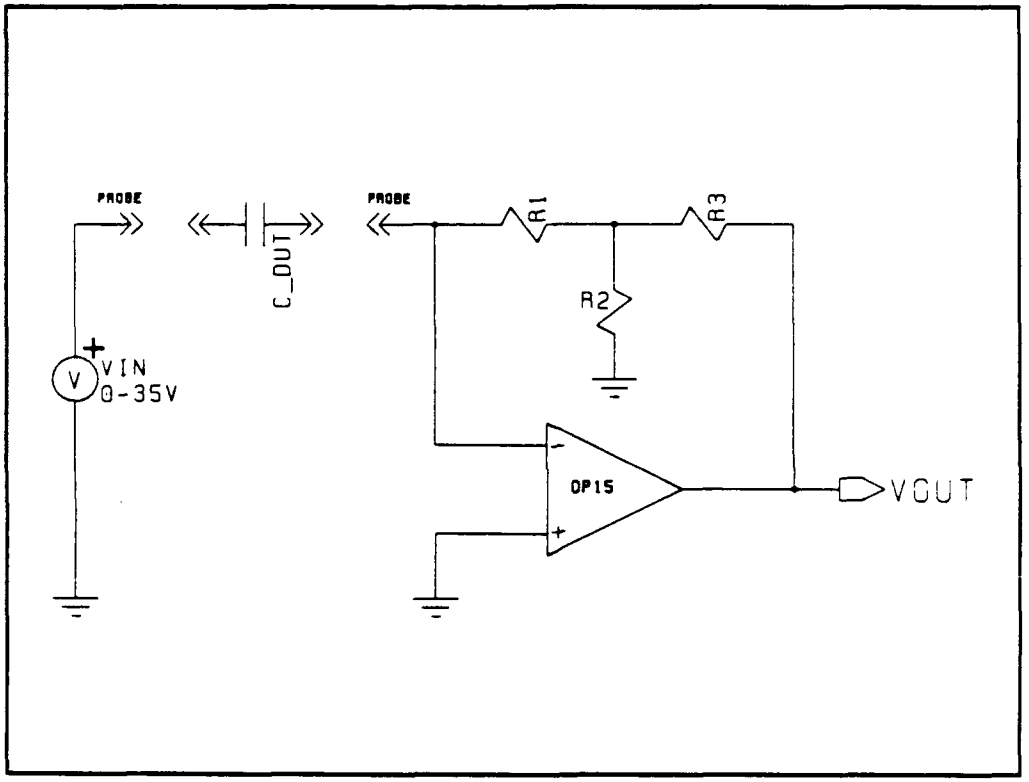


Figure 15 Oxide Characterization Test Fixture

Computer control of the testing environment was provided by an internally developed IEEE-488 bus controller program known as the Data Acquisition Environment (DAE). This program allows both interactive and automatic control of test equipment. In this investigation a series of "macro files" were created to allow a row of capacitors to be stepped through and tested automatically with the raw data stored in one common data file for later analysis. Appendix B contains a help file listing many of the important features of the DAE as well as some of the macro files created to control the test environment.

2.6 Results

Upon receiving the wafers which contained the oxide characterization test structures it was noted that the multiple stripe N-channel and P-channel devices both exhibited source to drain shorts. This was traced to gross over diffusion in both the n^+ and p^+ implants. As a result, the multiple stripe transistors were not able to provide us with information on the effective areas of the three gate oxide regions (gate to channel, gate to source overlap, and gate to drain overlap). Therefore testing was limited to the solid capacitors. The lot tested consisted of 900 solid substrate capacitors consisting of 300 from each size (size "a" = 4.0E-4 cm^2, size "b" = 8.0E-4 cm^2, size "c" = 1.6E-3 cm^2).

Due to limitations in the test setup we performed only voltage ramp tests where the capacitor voltage is steadily increased until the capacitor breaks down. No fixed voltage tests were performed to measure time to breakdown of the capacitors. The examples presented earlier in this section were taken from real data obtained during these tests. For completeness however all of the results are presented here. The input voltage to the capacitors was a ramp voltage with a ramp rate of approximately 100 Volts/second and was generated via a series of small discrete voltage steps. Figure 16 shows a typical input voltage waveform.

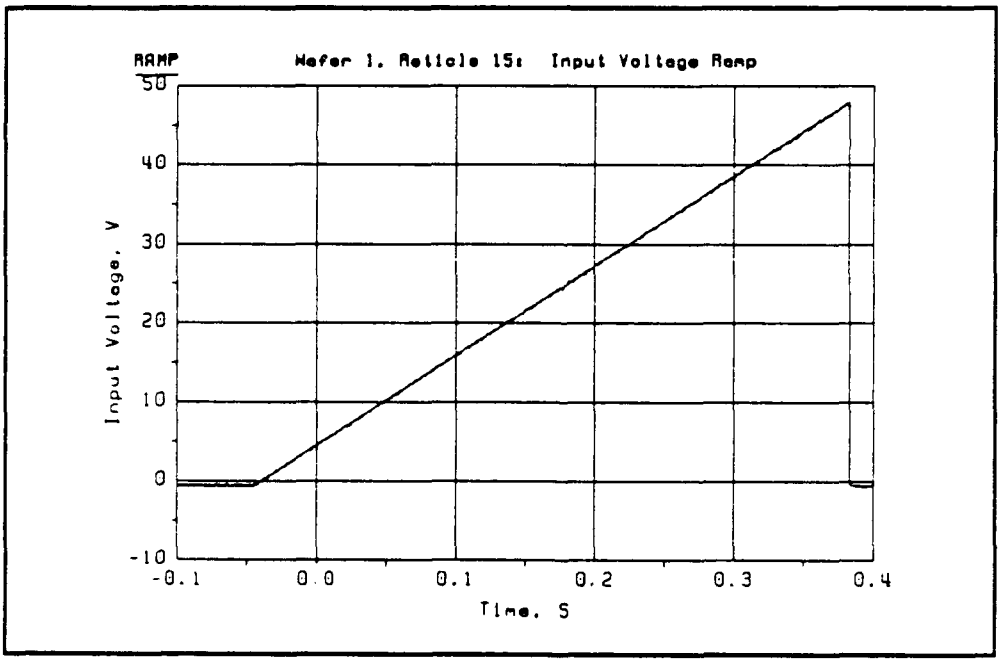


Figure 16 Sample Voltage Ramp Input Waveform

Figures 17 through 20 show the results from the lot of 300 size "a" capacitors. Figures 21 through 24 show the results from the lot of 300 "b" capacitors. Finally, figures 25 through 28 show the results from the lot of 300 size "c" capacitors.

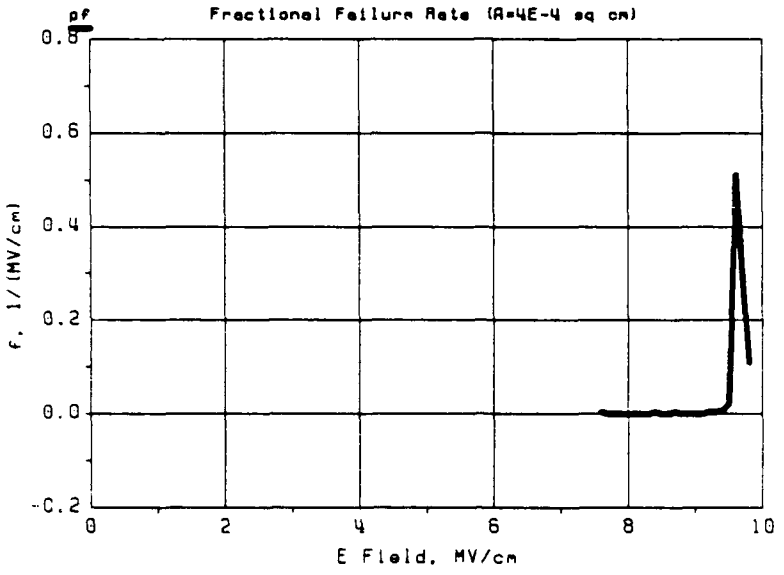


Figure 17 Size "A": Instantaneous Failure Rate

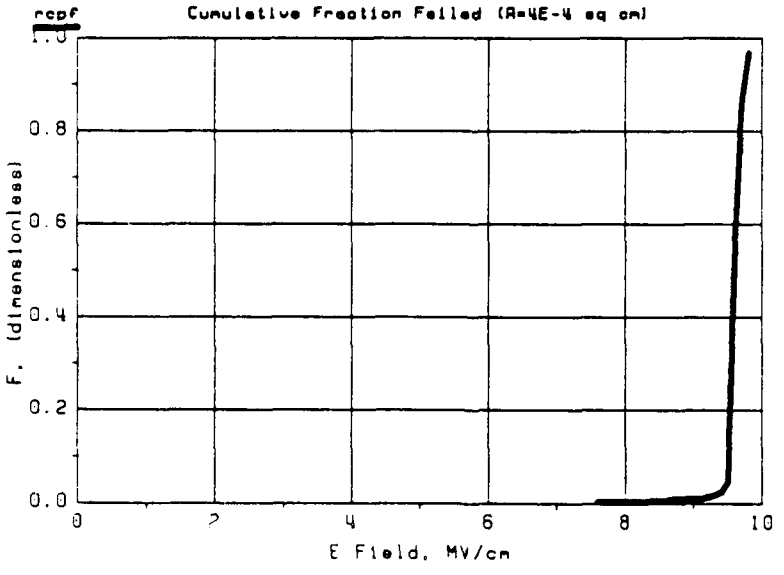


Figure 18 Size "A": Raw Cumulative Percent Failed

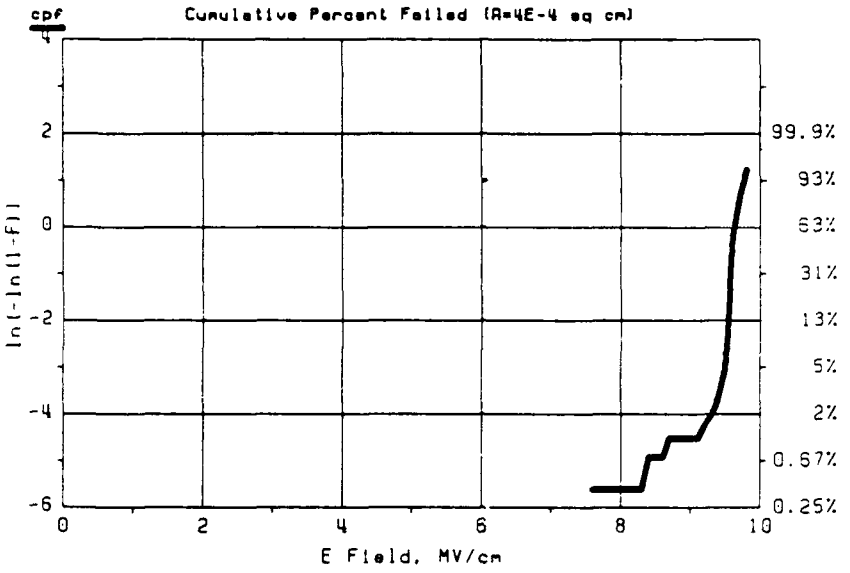


Figure 19 Size "A": Cumulative Percent Failed

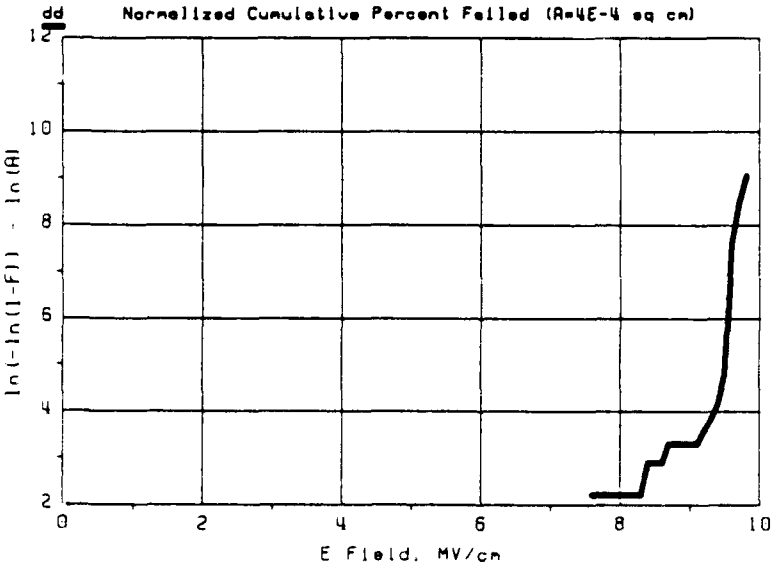


Figure 20 Size "A": Normalized Cumulative Percent Failed

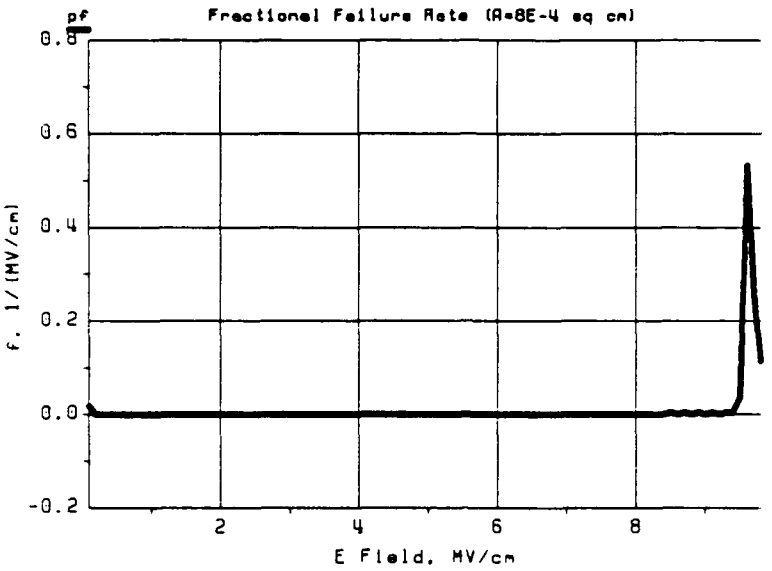


Figure 21 Size "B": Instantaneous Failure Rate

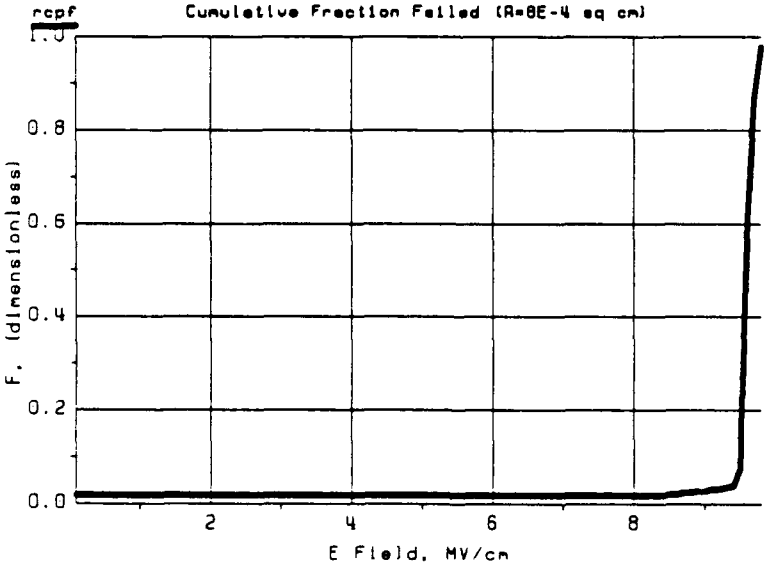


Figure 22 Size "B": Raw Cumulative Percent Failed

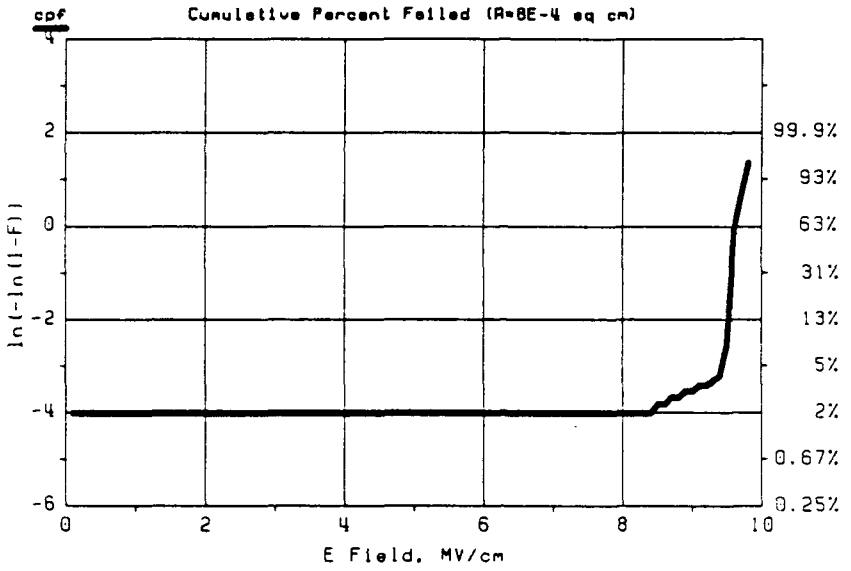


Figure 23 Size "B": Cumulative Percent Failed

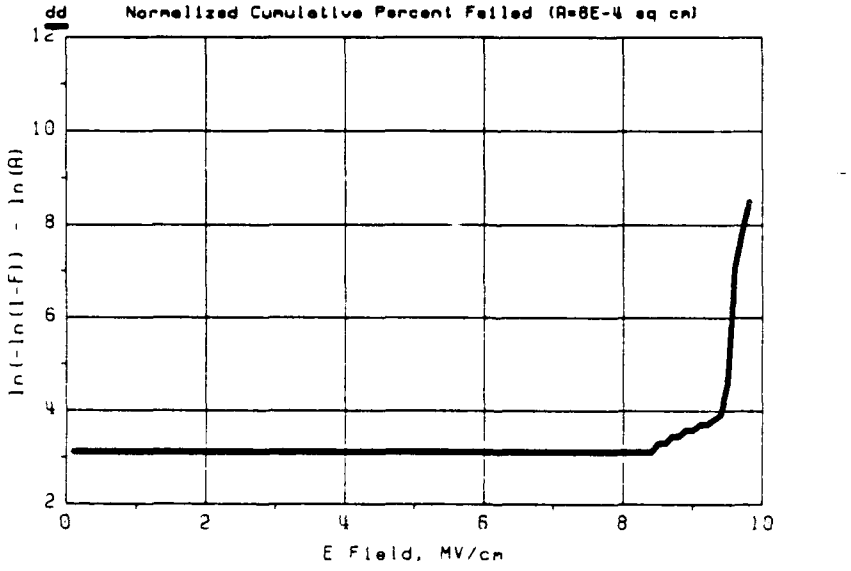


Figure 24 Size "B": Normalized Cumulative Percent Failed

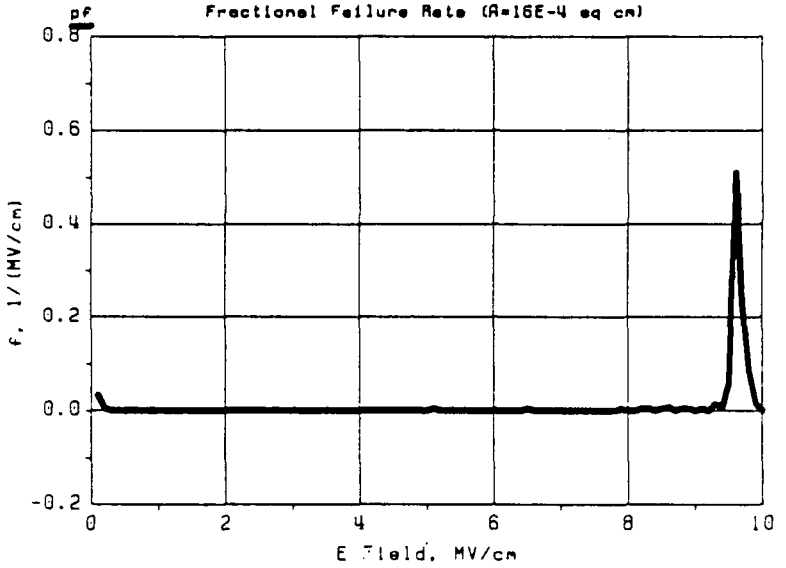


Figure 25 Size "C": Instantaneous Failure Rate

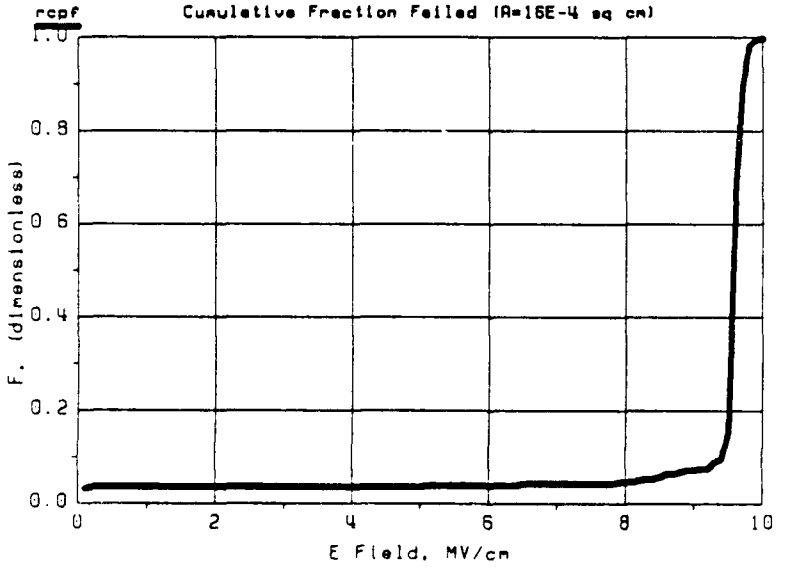


Figure 26 Size "C": Raw Cumulative Percent Failed

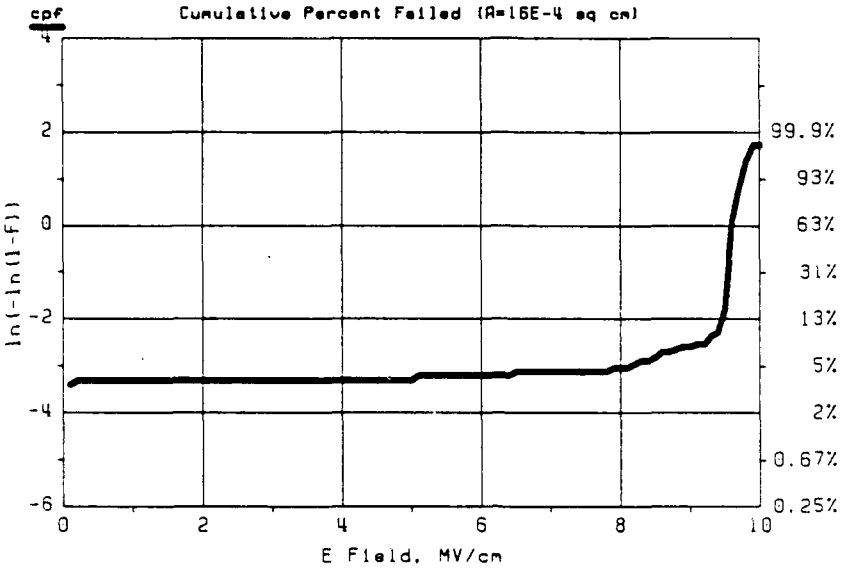


Figure 27 Size "C": Cumulative Percent Failed

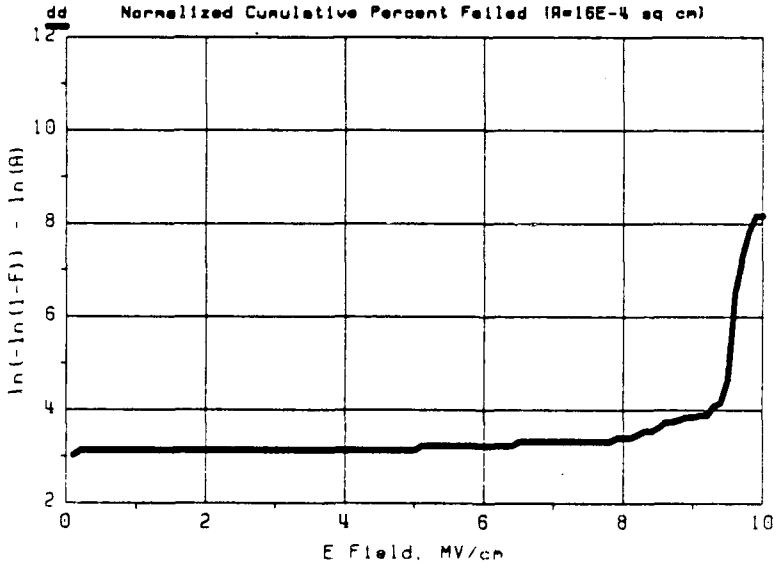


Figure 28 Size "C": Normalized Cumulative Percent Failed

Finally figure 29 displays the defect density results from the combined capacitor lots after accounting for the area effect. The resulting defect density equation for the capacitor's gate oxide before intrinsic breakdown (0.1 to 7.5 MV/cm) is:

$$\ln(\text{Defect density}) = (0.014)x + (3.10)\ \text{cm}^{-2}.$$

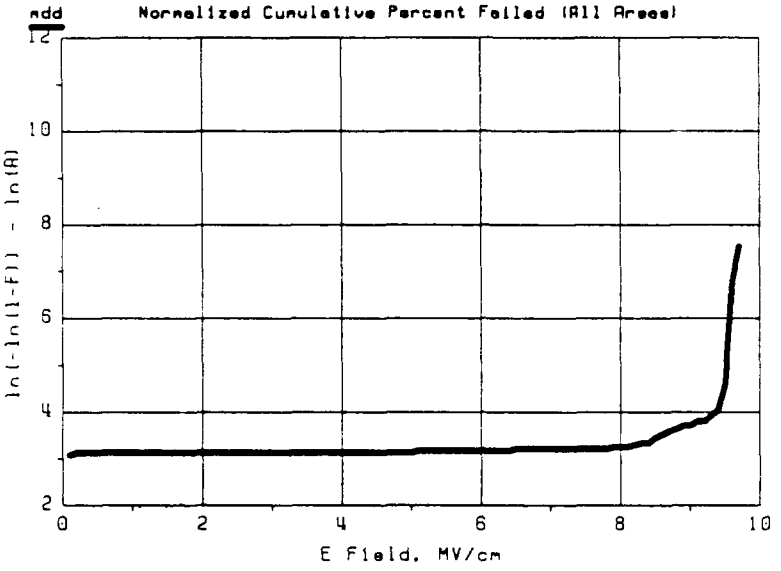


Figure 29 All Capacitors Combined: Log Defect Density

If we assume that the defect density of the test capacitor gate oxide is similar to that of the test vehicles we can calculate theoretical instantaneous failure rate curves for the test vehicles (assuming we could somehow apply the same ramp voltage to the test vehicle gate oxide). Given a gate oxide area of 9.2E-3 cm^2 for Test Vehicle B and 6.2E-3 cm^2 for Test Vehicle C we have:

$$\text{CPF (TVB)} = (0.014)x + (-1.59)\ \text{cm}^{-2}.$$

$$\text{CPF (TVC)} = (0.014)x + (-1.98)\ \text{cm}^{-2}.$$

The instantaneous failure rates of the test vehicles based on these equations are plotted in figures 30 and 31. These curves indicate that a 5 volt stress applied to all the gate oxides of the test vehicles (which corresponds to a 2.5 MV/cm stress given the test vehicles 225 Angstrom oxide) would screen out roughly 72% of the failures before intrinsic breakdown.

Although the present work did not address a method to determine voltage and time requirements for a device screen with fixed voltage from test structure tests with ramped voltage stress, the reader is referred to references 6 and 7, (cited in Section 1.4, pg. 16).

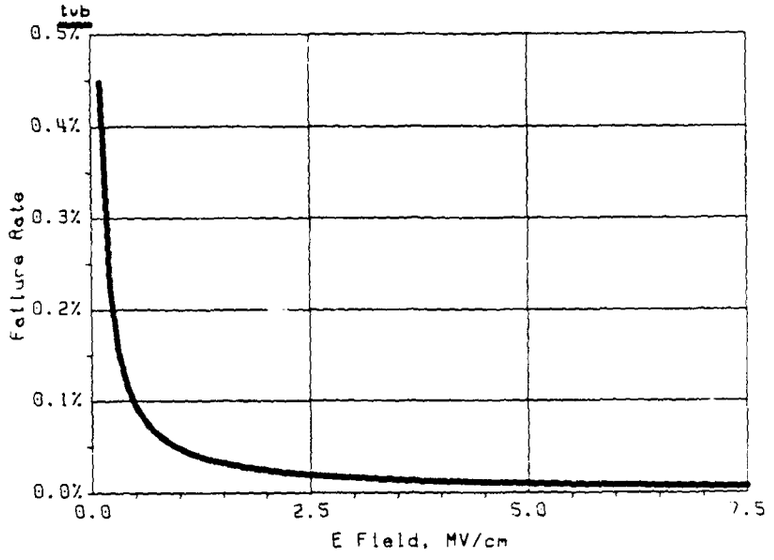


Figure 30 Test Vehicle B, Instantaneous Failure Rate

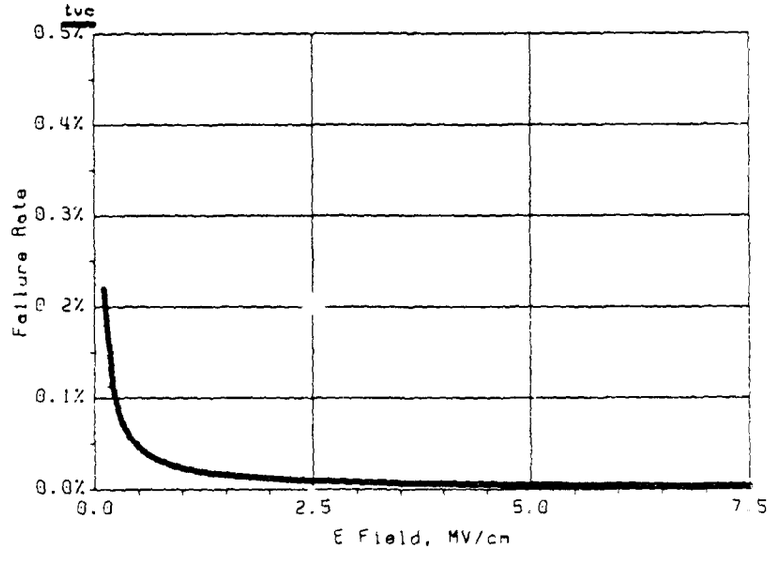


Figure 31 Test Vehicle C, Instantaneous Failure Rate

3. Internal Electrical Screening Methods

3.1 Background

In order to perform a screen on a complex digital circuit, it is of course necessary to apply the stress voltage to the gates of the transistors in the circuit. However, under the application of a normal test vector set, some gates in the circuit will receive far more stress than others. This may become a problem during screening if the process of applying sufficient stress to one gate in the circuit causes another gate to be unacceptably aged. The following two sections investigate methods for applying stress evenly to all gate oxides in a design.

One possible method of providing better gate oxide stress coverage during device screening is to incorporate special internal circuitry on a device. This internal circuitry serves to disable the normal logic functionality of the device and to enable a special mode in which the gate oxide may be more evenly stressed. In order to understand how to approach this task it is necessary to investigate somewhat deeper the problems involved in stressing the gate oxide of random logic devices.

It is perhaps easiest to begin with a couple of examples. The simplest logic element to consider is the inverter. Figure 32 shows the transistor diagram of a CMOS inverter. There are only two possible input states to consider: that when I1 is a logic one, and when I1 is a logic zero. Table 1 represents the stress received by all the gate oxide regions in this simple inverter.

The gate to drain overlap region of both transistors are stressed regardless of the state of input I1. This is due to the logic functionality of the inverter whereby the output O1 (the drain of both transistors) is always in the opposite logic state as the input I1 (the gate of both transistors.) As a result, the two sides of the gate to drain overlap region for both transistors are always in opposite logic states and are thus always being stressed. In contrast the gate to substrate and gate to source overlap regions are stressed only when each transistor turns on. Thus these two regions of the N-channel transistor are stressed when the input I1 is a logic one and these two regions of the P-channel transistor are stressed when the input I1 is a logic zero. Thus in the case of an inverter, if the input is generated randomly, a small portion of the gate oxide (the gate to drain overlap region) is stressed 100% of the time while the rest of the gate oxide is stressed 50% of the time.

Consider now the case of a two input NAND. Figure 33 shows the transistor diagram of a CMOS NAND. There are now four different input states which must be analyzed to determine the stress coverage possible for this device. Table 2 represents the stress received by all the gate oxide regions in this simple NAND element.

In this case, if the inputs are generated randomly, the gate to source overlap and the channel regions will be stressed 25% to 50% of the time while the gate to drain overlap region will be stressed 50% to 75% of the time. However, if there were a way to ensure that the two inputs I1 and I2 were always in like states (both a logic one or both a logic zero) the stress coverage would be quite similar to that of the inverter. The only difference in fact would be one gate to

drain overlap region which would be stressed 50% of the time rather than 100% of the time. Thus to evenly stress a simple inverting gate such as a NAND or a NOR, it is necessary to keep the inputs to the logic gate in like states.

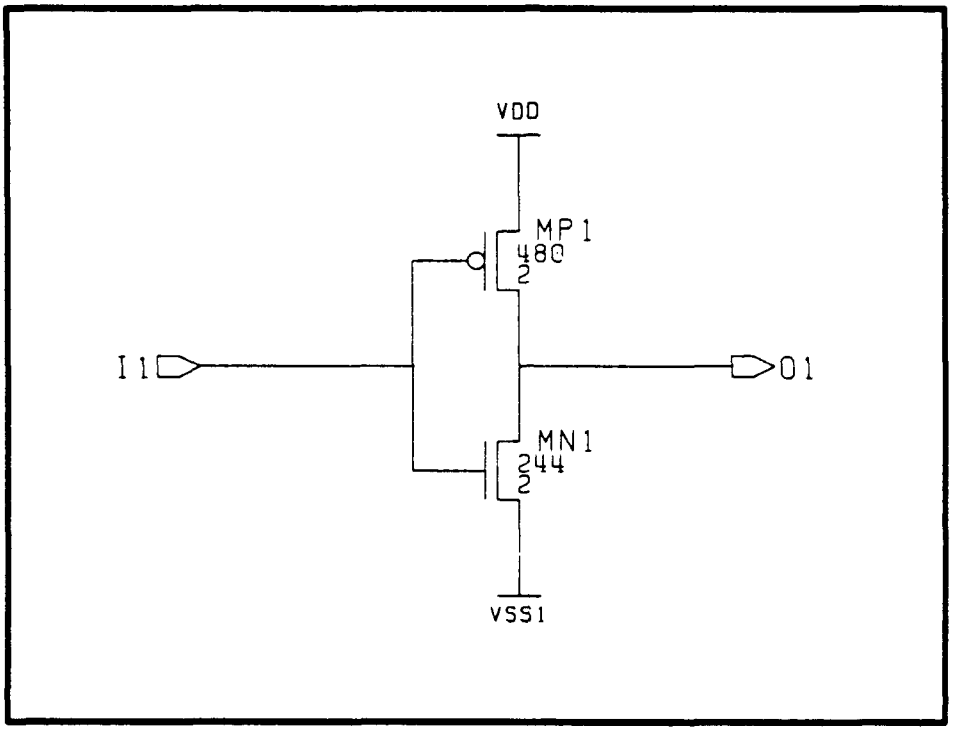


Figure 32 CMOS Inverter Transistor Schematic

PINS		MN1			MP1		
I1	O1	C	S	D	C	S	D
0	1	0	0	1	1	1	1
1	0	1	1	1	0	0	1

TABLE 1 CMOS Inverter Stress Matrix

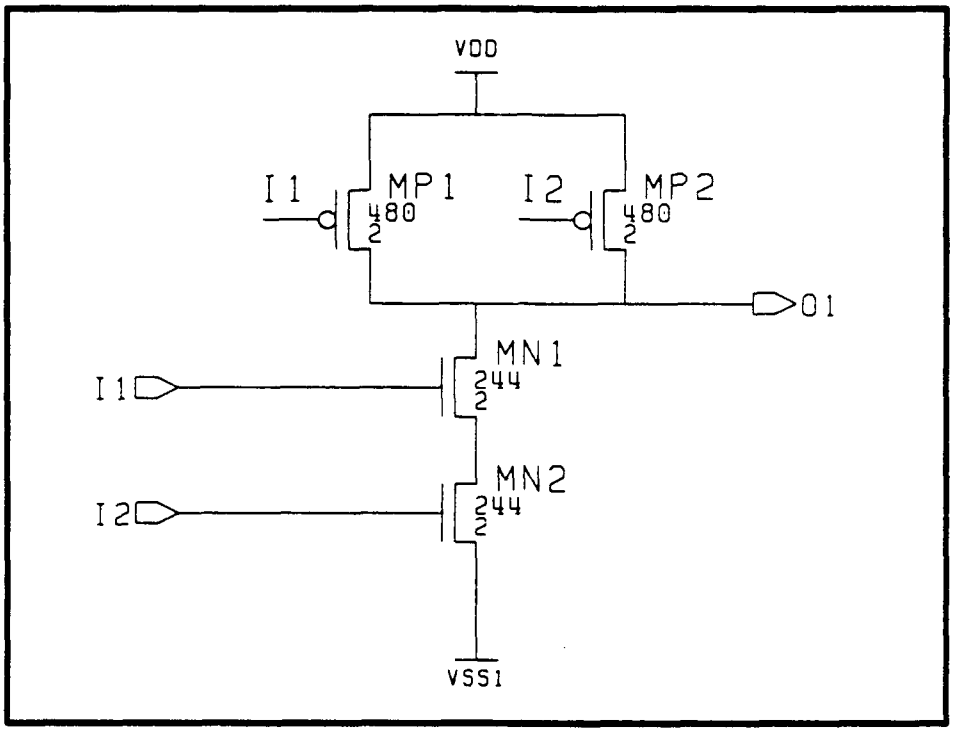


Figure 33 CMOS 2-Input NAND Transistor Schematic

PINS			MN1			MN2			MP1			MP2		
I1	I2	O1	C	S	D	C	S	D	C	S	D	C	S	D
0	0	1	0	*	1	0	0	*	1	1	1	1	1	1
0	1	0	0	0	1	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0	1	1	1
1	1	0	1	1	1	1	1	1	0	0	1	0	0	1

*** Node is floating: Oxide area is not stressed.**

TABLE 2 CMOS 2-Input NAND Stress Matrix

3.2 Internal Screening Circuitry

The functionality of a random logic circuit to a large degree prohibits toggling all inputs of the internal gates together. No matter how carefully a test vector set is designed, there is a limit on how evenly the stress can be applied to the various gate oxide regions on the device. This situation is illustrated in figures 34 through 35. Figure 34 shows a simple 3 to 8 decoder circuit with enable. Since there are only four separate inputs, there are 16 possible input vectors. Although it is easy to evenly stress the input inverters, the functionality of the decoder precludes even stressing of the rest of the circuit (particularly the NAND gates.)

Figure 35 is a histogram showing the stress received by the various oxide regions in the design. This figure displays total oxide area on the y-axis as a function of stress duty cycle on the x-axis. As can be seen from this figure, the 3 to 8 decoder cannot be very evenly stressed regardless of the combination of input vectors used. In order to achieve an even gate oxide stress, it is necessary to decouple the logic gates from one another and force their inputs high and low in unison using some other means. On this project it was decided to use the scheme shown in figure 36.

In this scheme, it is necessary to break down the logic design into simple logic gates which represent "inverting transistor clusters." An inverting transistor cluster is a simple pulldown transistor network and its accompanying complementary pullup network. Thus an inverter, NAND, or NOR gate is an inverting transistor cluster while an AND or OR gate are actually two clusters connected in series. For simplicity, the phrase "logic gate" should be considered to mean "inverting transistor cluster" in this report unless otherwise stated.

In this internal stressing scheme, four transistors are interposed between the output of every logic gate and the inputs which it drives. Transistors QA and QB which are controlled by signals SA and SB provide the means for decoupling the inputs of a gate from the output which drives them. Transistors QC and QD which are controlled by signals SC and SD provide the means to independently pull the logic gate's inputs high or low as required to provide even stress.

By holding SA high and SB low, all logic gates in the design are completely isolated from each other. This allows the gate oxide regions of each logic gate to be stressed evenly by first turning on the P-channel FET controlled by SC and then the N-channel FET controlled by SD. The remainder of the oxide area (gate to substrate of QA and QB) can then be stressed by turning on transistors QA and QB while QC and QD are turned off.

To illustrate this, figure 37 is a stress histogram for the 3 to 8 decoder of figure 34 with the internal stress scheme implemented. Note that there is a smaller spread in the amount of stress received by the gate oxide areas than in the previous histogram shown in figure 35 where the internal stressing scheme is not implemented.

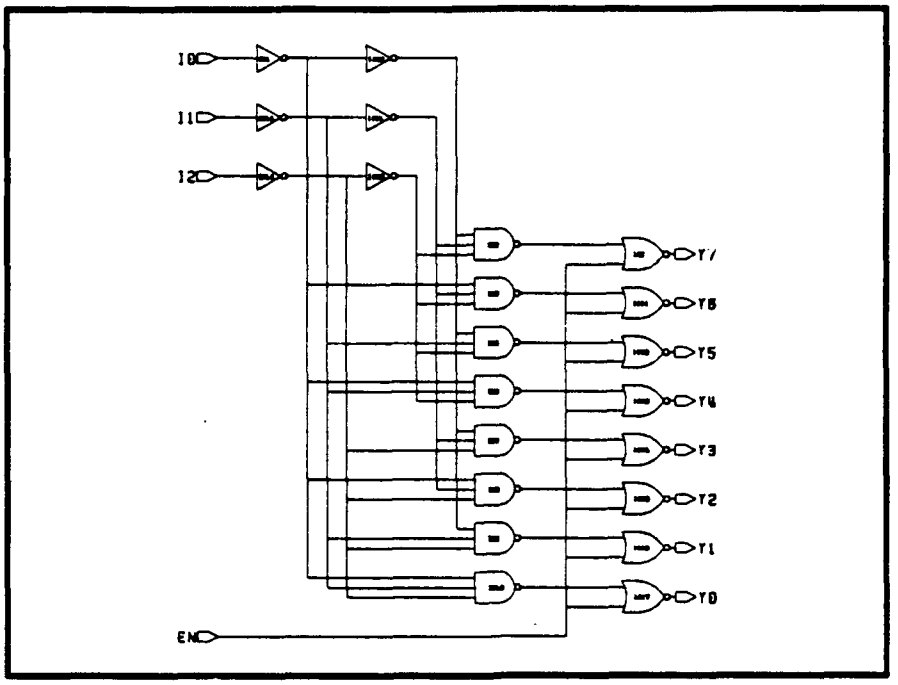


Figure 34 3-to-8 Decoder Gate Level Schematic

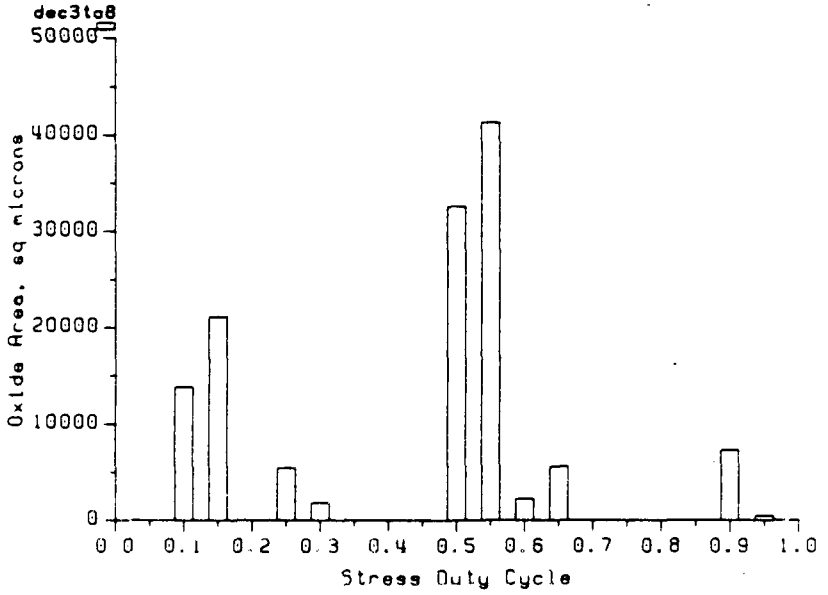


Figure 35 Sample Stress Histogram for 3-to-8 Decoder

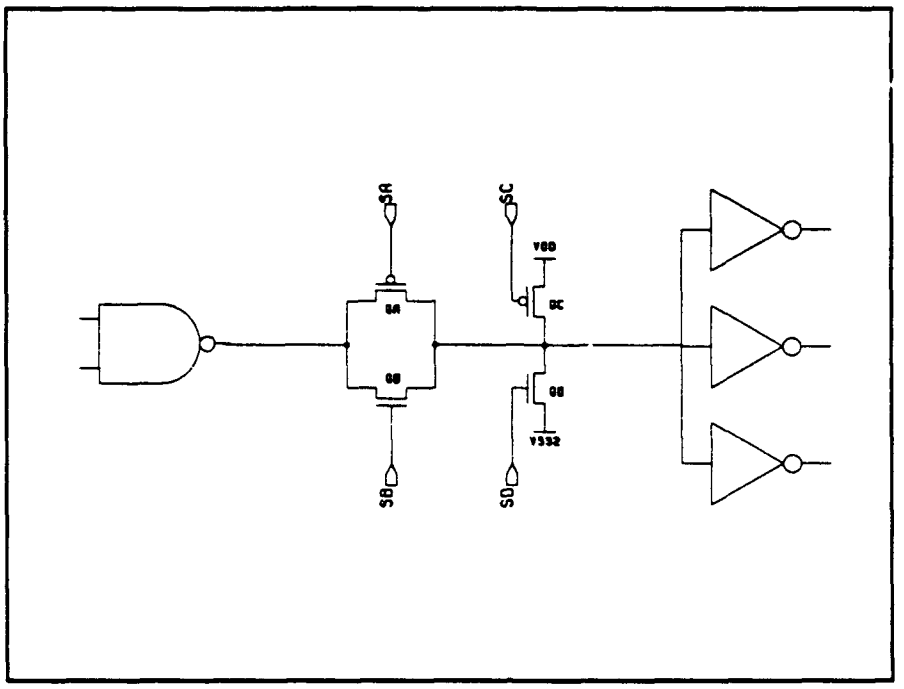


Figure 36 Internal Logic Decoupling and Stress Scheme

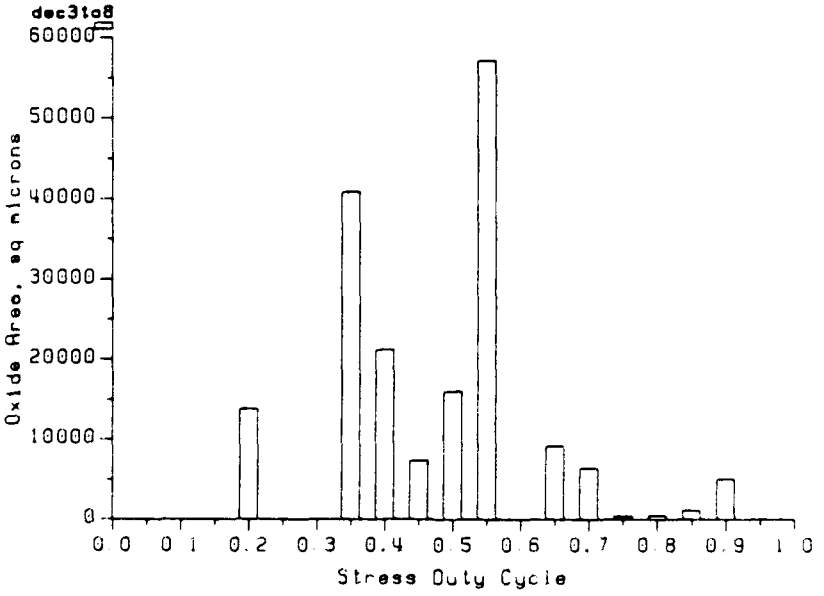


Figure 37 3-to-8 Decoder Stress Histogram with Decoupling Scheme Implemented

3.3 Stress Histograms

At this point it may be wise to diverge and briefly discuss the stress histograms used in the previous discussion. In order to quantitatively compare the effectiveness of an internal stressing scheme or of various test pattern sets at evenly stressing the gate oxide regions of a design it is necessary to record and analyze the stress received by each individual gate region during a logic simulation. We have divided this task into two phases: recording the stress received, and analyzing this stress data. The first task, recording of the stress received by each individual gate oxide region is performed by special Behavioral Language Models (BLMs) which drive the logic simulator for each logic gate. The operation of these BLMs will be covered in detail in section 5.

The analysis of the stress data is handled by the Oxide Stress Analyzer (OSA) which was first discussed in section 2. The simplest of these analyses are the stress histogram plots used in the previous section. To create these plots the OSA sorts through all the gate oxide regions in the design and separates them into "bins" depending on the stress duty cycle each region received. When this sorting procedure is complete, the OSA then adds up the total gate oxide area in each of the bins. Once this is done, the resulting data may be examined to determine the amount of gate oxide in the design which receives any given amount of stress. In addition, this data may be plotted to observe the relation between the amount of stress received and the total area of the gate oxide receiving that stress for every stress "bin."

This stress histogram may also be analyzed to determine the mean stress duty cycle as well as the standard deviation about the mean. This gives a quantitative measure of how evenly the design is being stressed. For example consider again the two stress histograms shown in figures 35 and 37. The mean of figure 35 is 0.42 and the standard deviation is 0.23. In contrast, figure 37 has a mean of 0.45 and a standard deviation of 0.15. This shows quantitatively that the 3 to 8 decoder is stressed more evenly when the internal stress scheme is implemented. Also of note is the fact the without the internal stress scheme implemented, the ratio of highest to lowest stress duty cycle is about 10. However, with the internal stress scheme this ratio is reduced to only 5. Therefore with the internal stress scheme, we would be roughly twice as effective developing a screening program which would stress all the oxide areas without significantly aging any oxides.

There is one more important use for the stress histogram data. Once the oxide areas have been sorted into their appropriate bins based on the amount of stress they received, the total oxide area in each bin may be treated as one homogeneous oxide area. This enables one to perform failure rate calculations for that bin based on the stress voltage chosen. The failure rate curves calculated for each bin may then be simply added together to arrive at a failure rate curve for the device as a whole.

Calculation of a failure rate curve for a device in this manner depends on the fact that the failure rate for a stress bin may be calculated using the total oxide area of the bin. If this were not the case, each individual gate oxide area would have to be considered independently. Calculating the failure rate for a bin as a whole requires that:

$$f(A+B+C+...) = f(A) + f(B) + f(C) + ... ,$$

where f is the failure rate while A, B, C, ... are the areas of the different oxide regions in the bin. This relationship may be proven in the following way.

Given two gate oxides with areas A_1 and A_2 respectively, we first calculate the probabilities of A_1 and A_2 respectively failing (F_1 and F_2). We know that the defect density (D) is given by the equation

$$D = 1/A \ln(1 - F)^{-1}$$

and thus

$$F = 1 - e^{-AD}$$

Therefore, for our oxides:

$$F_1 = 1 - e^{-A_1 D}$$

$$F_2 = 1 - e^{-A_2 D}$$

Now we must calculate the probability that either or both areas fail. In order to do this we must recall some definitions from probability theory.

$P(\xi_1 + \xi_2) \equiv$ probability of either or both ξ_1 or ξ_2 occurring.

$P(\xi_1 \cdot \xi_2) \equiv$ probability of both ξ_1 and ξ_2 occurring.

$P(\bar{\xi}_1 \cdot \bar{\xi}_2) \equiv$ probability of neither ξ_1 nor ξ_2 occurring.

We may then easily derive an identity for the probability of either or both events ξ_1 or ξ_2 occurring.

$$P(\xi_1 \cdot \xi_2) = P(\xi_1) \cdot P(\xi_2)$$

$$P(\bar{\xi}_1 \cdot \bar{\xi}_2) = P(\bar{\xi}_1) \cdot P(\bar{\xi}_2) = [1 - P(\xi_1)]\,[1 - P(\xi_2)]$$

$$P(\xi_1 + \xi_2) = 1 - P(\bar{\xi}_1 \cdot \bar{\xi}_2) = 1 - [1 - P(\xi_1)]\,[1 - P(\xi_2)]$$

This last expression is what we need to calculate the probability of either or both oxide areas failing. We will call this probability F_3.

$$F_3 = 1 - (1 - F_1)(1 - F_2)$$

$$F_3 = 1 - e^{-A_1 D}\, e^{-A_2 D}$$

$$F_3 = 1 - e^{-(A_1 + A_2)D}$$

By inspection, this last expression is simply the probability of the combined oxide with area $(A_1 + A_2)$ failing. Thus our method of grouping oxide areas into bins and then using the total oxide area in the bin to calculate a failure rate is correct.

As a final note, the OSA also can provide a list of the N least stressed and N most stressed gate oxide regions in the design. This information is very useful in ensuring that all oxide regions receive at least some stress from the test pattern set. As we will see in the following section this information is essential when developing a test pattern set for use in externally applied oxide stress.

4. External Electrical Screening Methods

4.1 Background

By far the most straightforward method for applying stress to the oxide area in a design is via an externally applied test pattern set which has been specifically optimized for this purpose. This technique removes the burden of screening for oxide defects from the chip designer and places it squarely on the shoulders of the test engineer. The test engineer must take an initial functional test pattern set and optimize it in order to achieve the most even stress possible. As a concrete example of the external screening method, recall the previous example of a 3-to-8 decoder. A sample stress histogram for this circuit was shown in Figure 35. The Oxide Stress Analyzer (OSA) contains special features which aid in the process of optimizing a test vector set for even oxide stress.

4.2 Optimization Tools

The first OSA feature which aids the test vector optimization task is the "N most" and "N least" commands. Using these commands, the OSA is able to examine the stress history of a circuit when exercised with a given test pattern and generate a list of the N most stressed and N least stressed areas in a design. This list may then be used to add or remove test vectors in order to even the stress duty cycle in problem areas of the circuit. An example output from the "N least" command is shown below.

```
 1:  Instance "/i$2/i$2"
        Transistor "mp2"
           Length:  2
           Width:  480
              Source:
                 Area:  96
                 Stress:  0.06

 2:  Instance "/i$2/i$2"
        Transistor "mp2"
           Length:  2
           Width:  480
              Channel:
                 Area:  768
                 Stress:  0.06

              .
              .
              .


17:  Instance "/i$2/i$4"
        Transistor "mn1"
```

```
            Length:  2
            Width:  244
               Source:
                  Area:  30.5
                  Stress:  0.12

 18:  Instance "/i$2/i$4"
         Transistor "mn1"
            Length:  2
            Width:  244
               Channel:
                  Area:  427
                  Stress:  0.12

                .
                .
                .
```

4.3 Detailed Stress Information

In addition, the behavioral language models (BLM's) used in simulating a circuit have the capability of keeping track of the stress received by all the oxide areas in a device on a vector by vector basis. This enables a more detailed analysis of the stress received by problem areas in the design. A vector by vector stress report for the 3-to-8 decoder is shown below. This vector by vector list of stress received by a design is in an ideal format to be used by an automated "test vector optimizer" computer program.

```
;
; File: state.dat
; Content: Record of applied stress during simulation of design "stresstest"
;          using pattern file "forcefile" on a vector by vector basis.
;


  #
  # Ordered list of oxide areas in design...
  #
  /I$2/I$22/MN1/G-427.00  ,
  /I$2/I$22/MN1/D-30.50   ,
  /I$2/I$22/MN1/S-30.50   ,
             .
             .


  /I$2/I$17/MP2/G-768.00  ,
  /I$2/I$17/MP2/D-96.00   ,
```

```
  /I$2/I$17/MP2/S-96.00    ;
/ 0 /
  #
  # Ordered list of stress received during vector 0...
  #
  /I$2/I$22-111010,
  /I$2/I$21-111010,
  /I$2/I$20-111010,
  /I$2/I$1-010111,
  /I$2/I$18-010111,
  /I$2/I$19-010111,
  /I$2/I$3-010000000111111111,
  /I$2/I$4-000010000000111111,
  /I$2/I$5-010000000111000111,
  /I$2/I$6-000000010000000111,
  /I$2/I$7-010000111111111000,
  /I$2/I$8-000010111000111000,
  /I$2/I$9-010111111111000000,
  /I$2/I$10-111111111010010010,
  /I$2/I$2-111000010000,
  /I$2/I$11-111000010000,
  /I$2/I$12-111000010000,
  /I$2/I$13-111000010000,
  /I$2/I$14-111000010000,
  /I$2/I$15-111000010000,
  /I$2/I$16-111000010000,
  /I$2/I$17-010010111111;
/ 1 /
  #
  # Ordered list of stress received during vector 1...
  #
  /I$2/I$22-111010,
  /I$2/I$21-111010,
  /I$2/I$20-111010,
  /I$2/I$1-010111,
  /I$2/I$18-010111,
  /I$2/I$19-010111,
  /I$2/I$3-010000000111111111,
  /I$2/I$4-000010000000111111,
  /I$2/I$5-010000000111000111,
  /I$2/I$6-000000010000000111,
  /I$2/I$7-010000111111111000,
  /I$2/I$8-000010111000111000,
  /I$2/I$9-010111111111000000,
  /I$2/I$10-111111111010010010,
  /I$2/I$2-111000010000,
  /I$2/I$11-111000010000,
```

```
  /I$2/I$12-111000010000,
  /I$2/I$13-111000010000,
  /I$2/I$14-111000010000,
  /I$2/I$15-111000010000,
  /I$2/I$16-111000010000,
  /I$2/I$17-010010111111;
            .
            .
            .

/ 47 /
  #
  # Ordered list of stress received during vector 47...
  #
  /I$2/I$22-010111,
  /I$2/I$21-010111,
  /I$2/I$20-010111,
  /I$2/I$1-111010,
  /I$2/I$18-111010,
  /I$2/I$19-111010,
  /I$2/I$3-111111111010010010,
  /I$2/I$4-010111111111000000,
  /I$2/I$5-000010111000111000,
  /I$2/I$6-010000111111111000,
  /I$2/I$7-000000010000000111,
  /I$2/I$8-010000000111000111,
  /I$2/I$9-000010000000111111,
  /I$2/I$10-010000000111111111,
  /I$2/I$2-000111111010,
  /I$2/I$11-111111000010,
  /I$2/I$12-111111000010,
  /I$2/I$13-111111000010,
  /I$2/I$14-111111000010,
  /I$2/I$15-111111000010,
  /I$2/I$16-111111000010,
  /I$2/I$17-111111000010;
```

4.4 A Stress Optimization Example

To better understand the process involved in using these tools to optimize a test pattern set for even stress, consider a simple three gate example. The gate level schematic for this circuit is shown in Figure 38 below. Since this circuit has only n inputs, it is easiest to begin with a pattern set which simply contains each possible combination of inputs. The stress histogram for this pattern set is shown in Figure 39. Following this is the stress history file used to create the histogram. This file is a record of the stress duty cycle of each oxide area in the design.

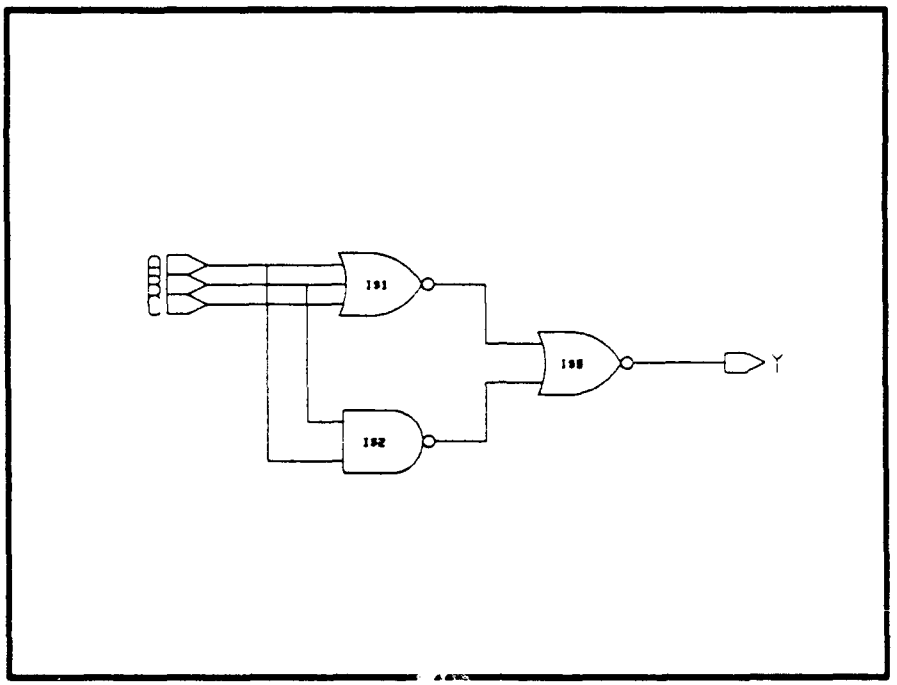


Figure 38 A Simple Three Gate Example Circuit

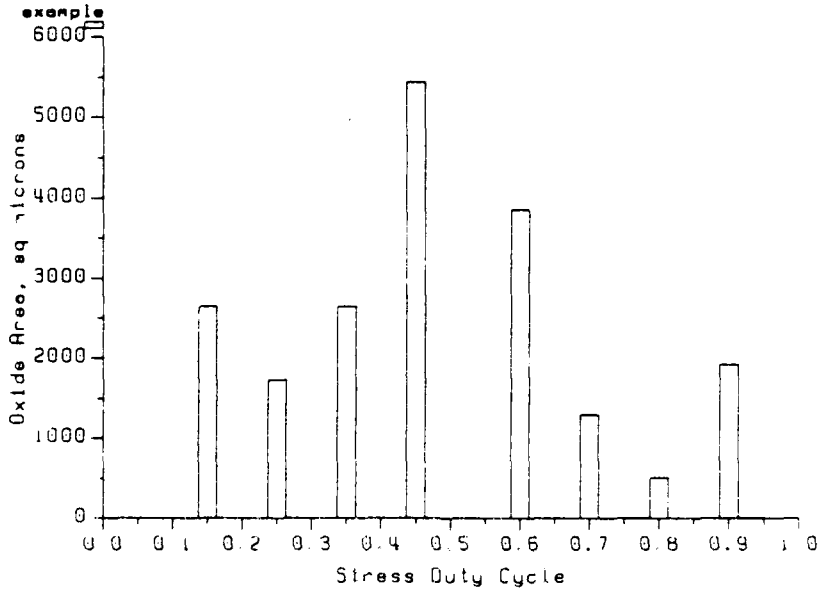


Figure 39 Initial Uneven Stress Histogram

```
;
; File: stress.dat
; Content: Record of applied stress during simulation of design "stresstest"
;          using pattern file "forcefile".
;
; Format of each instance record:
;
;(instance
;   (name <instance>)
;   (type <gate_type>)
;   (pin (name <pin>) (stress <fraction_time_high>))
;                .
;                .
;                .
;
;   (pin (name <pin>) (stress <fraction_time_high>))
;   (transistor
;      (name <transistor_name>)
;      (length <gate_length>)
;      (width  <gate_width>)
;      (channel (area <channel_area>) (stress <fraction_time_stressed>))
;      (source  (area <source_area>)  (stress <fraction_time_stressed>))
;      (drain   (area <drain_area>)   (stress <fraction_time_stressed>)))
;                      .
;                      .
;                      .
;   (transistor
;      (name <transistor_name>)
;      (length <gate_length>)
;      (width  <gate_width>)
;      (channel (area <channel_area>) (stress <fraction_time_stressed>))
;      (source  (area <source_area>)  (stress <fraction_time_stressed>))
;      (drain   (area <drain_area>)   (stress <fraction_time_stressed>))))
;
;
;
;

(instance (name /I$2) (type NAND2)
   (pin (name I1) (stress     0.56))
   (pin (name I2) (stress     0.56))
   (pin (name O1) (stress     0.67))
   (transistor
      (name MN1)
      (length     2.00)
      (width    244.00)
```

```
      (channel (area   427.00) (stress     0.33))
      (source  (area    30.50) (stress     0.33))
      (drain   (area    30.50) (stress     0.78)))
   (transistor
      (name MN2)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     0.78)))
   (transistor
      (name MP1)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.44))
      (source  (area    96.00) (stress     0.44))
      (drain   (area    96.00) (stress     0.78)))
   (transistor
      (name MP2)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.44))
      (source  (area    96.00) (stress     0.44))
      (drain   (area    96.00) (stress     0.78))))

(instance (name /I$1) (type NOR3)
   (pin (name I1) (stress     0.56))
   (pin (name I2) (stress     0.56))
   (pin (name I3) (stress     0.56))
   (pin (name O1) (stress     0.11))
   (transistor
      (name MN1)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     0.67)))
   (transistor
      (name MN2)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     0.67)))
   (transistor
      (name MN3)
      (length     2.00)
```

```
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     0.67)))
   (transistor
      (name MP1)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.44))
      (source  (area    96.00) (stress     0.44))
      (drain   (area    96.00) (stress     0.56)))
   (transistor
      (name MP2)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.22))
      (source  (area    96.00) (stress     0.22))
      (drain   (area    96.00) (stress     0.44)))
   (transistor
      (name MP3)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.11))
      (source  (area    96.00) (stress     0.11))
      (drain   (area    96.00) (stress     0.67))))

(instance (name /I$3) (type NOR2)
   (pin (name I1) (stress     0.11))
   (pin (name I2) (stress     0.67))
   (pin (name O1) (stress     0.33))
   (transistor
      (name MN1)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.11))
      (source  (area    30.50) (stress     0.11))
      (drain   (area    30.50) (stress     0.44)))
   (transistor
      (name MN2)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.67))
      (source  (area    30.50) (stress     0.67))
      (drain   (area    30.50) (stress     1.00)))
   (transistor
      (name MP1)
      (length     2.00)
```

```
    (width     480.00)
    (channel (area    768.00) (stress      0.89))
    (source  (area     96.00) (stress      0.89))
    (drain   (area     96.00) (stress      0.89)))
 (transistor
    (name MP2)
    (length      2.00)
    (width     480.00)
    (channel (area    768.00) (stress      0.33))
    (source  (area     96.00) (stress      0.33))
    (drain   (area     96.00) (stress      1.00))))
```

It is obvious from this stress listing that the multiple input gates are causing some problems because the inputs are not being toggled high and low in tandem. Figure 40 is the stress histogram that results after the pattern set is modified so that the inputs are being driven high and low together. Following this is the stress history file for this improved vector set. The resultant stress is far more even than it was to begin with. It is only fair to mention that this example is not representative of all random logic. The 3-to-8 decoder which was used in some previous examples represents an important class of random logic circuits and is completely resistant to any attempts at optimization. In fact, an initial test vector set which simply tests the response of a decoder given all possible input combinations is guaranteed to achieve the best stress coverage possible.

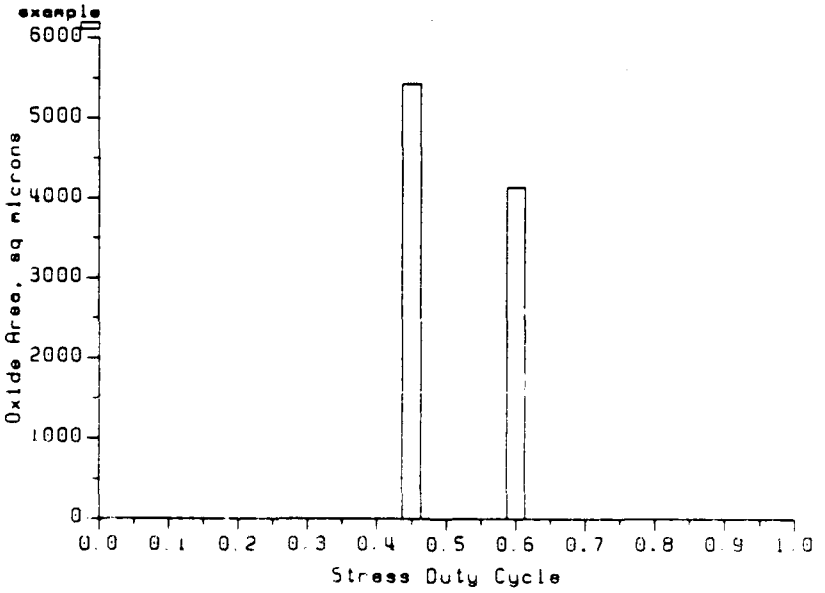


Figure 40 Stress Histogram of Modified Vector Set

```
;
; File: stress.dat
; Content: Record of applied stress during simulation of design "stresstest"
;          using pattern file "forcefile".
;
; Format of each instance record:
;
;(instance
;   (name <instance>)
;   (type <gate_type>)
;   (pin (name <pin>) (stress <fraction_time_high>))
;                .
;                .
;                .
;
;   (pin (name <pin>) (stress <fraction_time_high>))
;   (transistor
;      (name <transistor_name>)
;      (length <gate_length>)
;      (width  <gate_width>)
;      (channel (area <channel_area>) (stress <fraction_time_stressed>))
;      (source  (area <source_area>)  (stress <fraction_time_stressed>))
;      (drain   (area <drain_area>)   (stress <fraction_time_stressed>)))
;                      .
;                      .
;                      .
;   (transistor
;      (name <transistor_name>)
;      (length <gate_length>)
;      (width  <gate_width>)
;      (channel (area <channel_area>) (stress <fraction_time_stressed>))
;      (source  (area <source_area>)  (stress <fraction_time_stressed>))
;      (drain   (area <drain_area>)   (stress <fraction_time_stressed>))))
;
;
;
;

(instance (name /I$2) (type NAND2)
   (pin (name I1) (stress     0.56))
   (pin (name I2) (stress     0.56))
   (pin (name O1) (stress     0.44))
   (transistor
      (name MN1)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
```

```
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     1.00))
   (transistor
      (name MN2)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     0.56)))
   (transistor
      (name MP1)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.44))
      (source  (area    96.00) (stress     0.44))
      (drain   (area    96.00) (stress     1.00)))
   (transistor
      (name MP2)
      (length     2.00)
      (width    480.00)
      (channel (area   768.00) (stress     0.44))
      (source  (area    96.00) (stress     0.44))
      (drain   (area    96.00) (stress     1.00))))

(instance (name /I$1) (type NOR3)
   (pin (name I1) (stress     0.56))
   (pin (name I2) (stress     0.56))
   (pin (name I3) (stress     0.56))
   (pin (name O1) (stress     0.44))
   (transistor
      (name MN1)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     1.00)))
   (transistor
      (name MN2)
      (length     2.00)
      (width    244.00)
      (channel (area   427.00) (stress     0.56))
      (source  (area    30.50) (stress     0.56))
      (drain   (area    30.50) (stress     1.00)))
   (transistor
      (name MN3)
      (length     2.00)
      (width    244.00)
```

```
      (channel (area    427.00) (stress      0.56))
      (source  (area     30.50) (stress      0.56))
      (drain   (area     30.50) (stress      1.00)))
   (transistor
      (name MP1)
      (length      2.00)
      (width     480.00)
      (channel (area    768.00) (stress      0.44))
      (source  (area     96.00) (stress      0.44))
      (drain   (area     96.00) (stress      0.44)))
   (transistor
      (name MP2)
      (length      2.00)
      (width     480.00)
      (channel (area    768.00) (stress      0.44))
      (source  (area     96.00) (stress      0.44))
      (drain   (area     96.00) (stress      0.44)))
   (transistor
      (name MP3)
      (length      2.00)
      (width     480.00)
      (channel (area    768.00) (stress      0.44))
      (source  (area     96.00) (stress      0.44))
      (drain   (area     96.00) (stress      1.00))))

(instance (name /I$3) (type NOR2)
   (pin (name I1) (stress      0.44))
   (pin (name I2) (stress      0.44))
   (pin (name O1) (stress      0.55))
   (transistor
      (name MN1)
      (length      2.00)
      (width     244.00)
      (channel (area    427.00) (stress      0.44))
      (source  (area     30.50) (stress      0.44))
      (drain   (area     30.50) (stress      1.00)))
   (transistor
      (name MN2)
      (length      2.00)
      (width     244.00)
      (channel (area    427.00) (stress      0.44))
      (source  (area     30.50) (stress      0.44))
      (drain   (area     30.50) (stress      1.00)))
   (transistor
      (name MP1)
      (length      2.00)
      (width     480.00)
```

```
    (channel (area   768.00) (stress     0.56))
    (source  (area    96.00) (stress     0.56))
    (drain   (area    96.00) (stress     0.56)))
(transistor
    (name MP2)
    (length     2.00)
    (width    480.00)
    (channel (area   768.00) (stress     0.56))
    (source  (area    96.00) (stress     0.56))
    (drain   (area    96.00) (stress     1.00))))
```

4.5 Summary

In summary, the use of externally applied stress in screening for oxide defects is attractive since there are no chip performance or complexity penalties associated with its use. However, for a complex circuit it appears to be extremely difficult to optimize a test pattern set for even stress duty cycle.

5. Test Vehicle Design

5.1 Overview

Two test vehicles were designed and fabricated on this project. The first, known as Test Vehicle C (TVC) is a medium scale integration (MSI) random logic circuit very similar to the control decode section of a bit-slice microprogram sequencer. Test Vehicle B (TVB) is logically identical to TVC but incorporates the logic decoupling and stress scheme detailed in section 3. Detailed schematics of both test vehicles may be found in appendix C.

In order to conserve resources both test vehicles were fabricated on one monolithic substrate and packaged together in a single 48 pin ceramic dual in-line package (DIP). The top level schematic of the combined test vehicle is shown in figure 41. This combined packaging caused one problem since the test vehicles were required to operate entirely independent from each other in the event that one failed during the life test. Thus the test vehicles have independent VDD and VSS supplies but since they were fabricated in a CMOS P-well process, the VDD supplies are ties together via the n-type substrate. However, the VSS supplies are isolated from each other. This allows for the continued operation of one of the test vehicles if the other fails by simply disconnecting the VSS supply from the failed half of the chip.

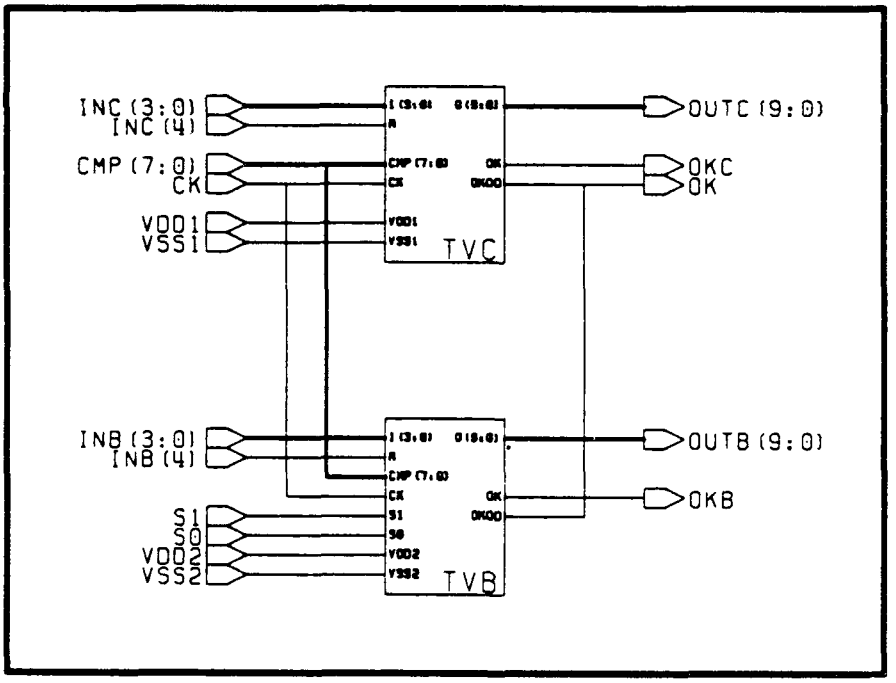


Figure 41 Combined Test Vehicle Schematic

Each test vehicle consists of two distinct areas:

1. MSI Combinatorial Logic: This is the main combinatorial logic which we are testing. In the case of Test Vehicle C it is the unmodified random logic design while in the

case of Test Vehicle B it is the same design which has been modified to include the internal screening circuitry. In both cases this logic is scaled up considerably in dimensions in order to create more gate oxide area. This is essential if we wish to achieve any gate oxide failures.

2. Health Monitoring Circuitry: In order to aid in dynamic monitoring during the life test, each test vehicle also includes some internal health monitoring circuitry. The heart of this circuitry is a comparator which is used to compare the actual outputs of the circuit with the expected outputs. If the actual outputs agree with the expected outputs the test vehicle reports that it is healthy. If the outputs do not compare, the test vehicle health monitor then reports that there is a problem. This allows for simple dynamic monitoring of the devices while in life test since most functional failures will be detected and reported by a single output pin.

   In addition to the comparator a transparent latch is included to allow the test vehicle health monitor to work properly in conjunction with a board level health monitor during the life test. Finally, the health monitor circuitry also contains an encoder circuit. This was dictated by packaging restrictions. There were not enough pins on the 48 pin DIP selected to allow a direct comparison of the test vehicle outputs with the expected outputs. By encoding the outputs somewhat we were able to do the comparison completely but with fewer pins. A simple schematic of this health monitoring circuitry is shown in figure 42.

   Figures 43 and 44 show the partitioning of the test vehicles into the combinatorial and health monitoring circuitry. Again, detailed schematics for the test vehicles may be found in appendix C.

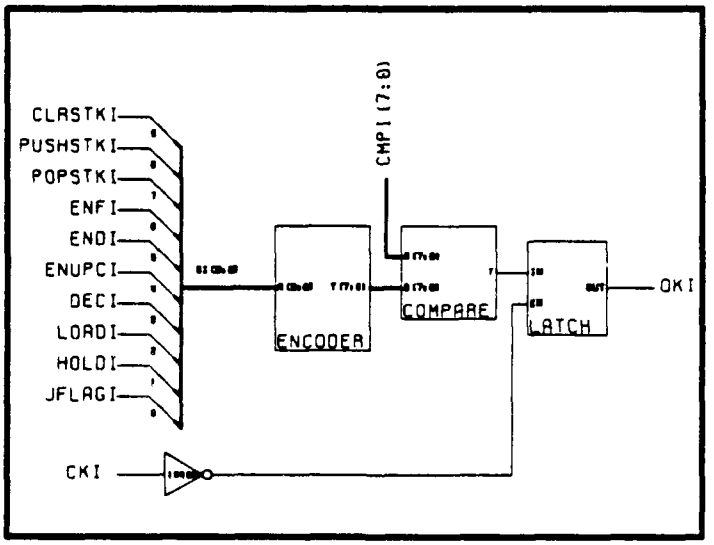


Figure 42 Health Monitor Circuitry Schematic

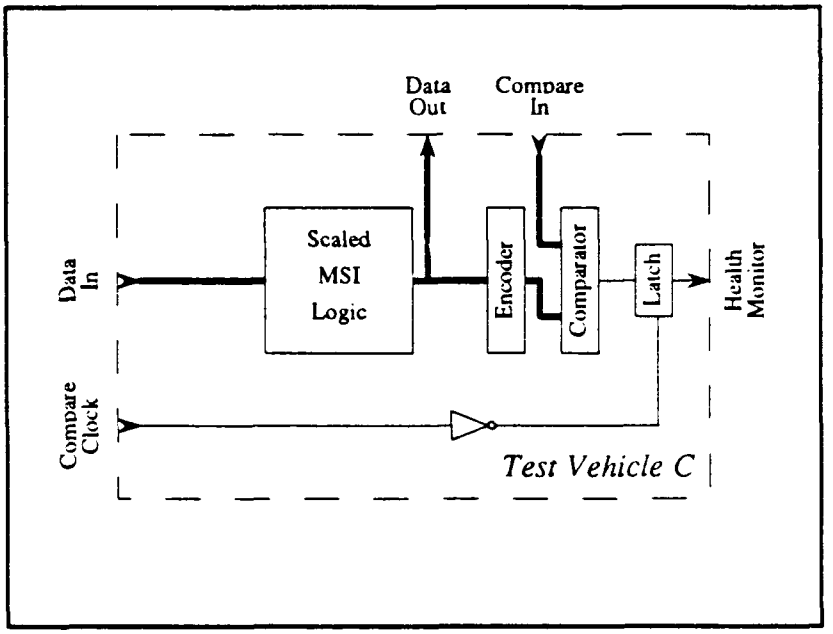


Figure 43 Test Vehicle C Logic Partitioning

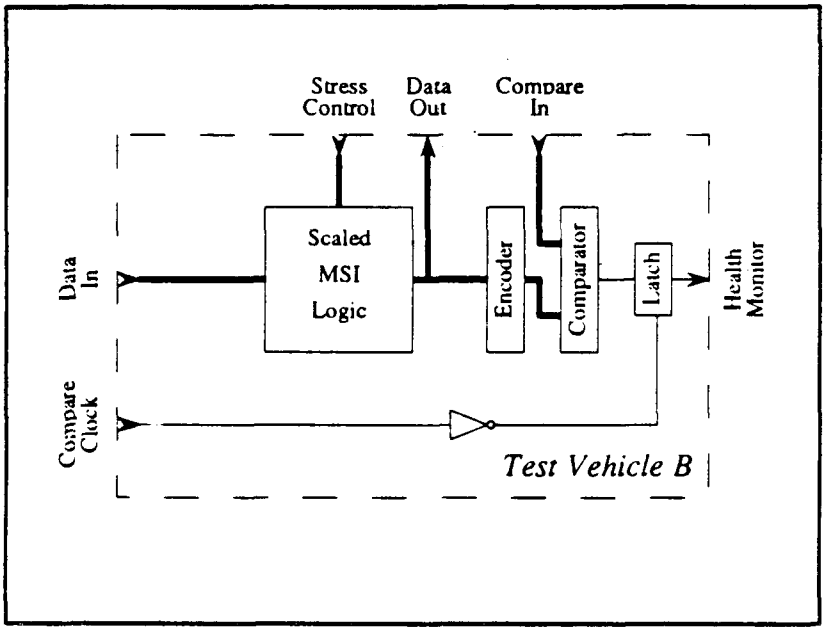


Figure 44 Test Vehicle B Logic Partitioning

All internal circuitry is scaled up in size by designing it using large, multiple stripe transistors in the basic cells. This is the same technique used when designing very large transistors for buffers or I/O pads. As a result, the design is still implemented using a 2 micron CMOS

process but the effective gate oxide area is substantially increased. This situation is illustrated in figure 45 which shows the physical layout of a simple inverter. Notice that each transistor is comprised of several transistors wired in parallel.

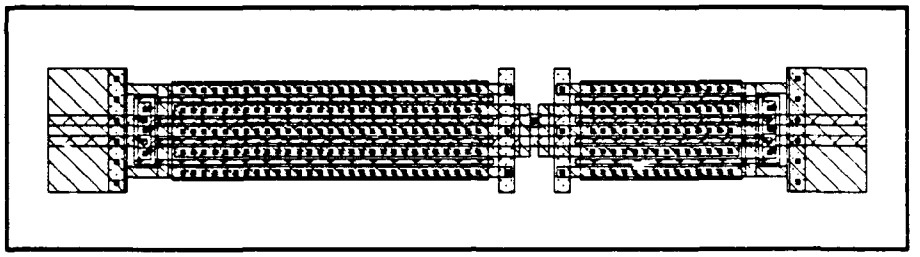


Figure 45 Multiple Stripe Inverter Layout

Figure 46 is a scanning electron microscope (SEM) photograph of the complete test vehicle. This photograph clearly shows that the die area is divided into three distinct sections. The top section of the die is Test Vehicle C and the bottom section is Test Vehicle B. Each of these test vehicles were designed as separate standard cell designs. All of the common inputs (CMP(7:0) and CK) as well as the one common open drain output (OK) are located directly opposing each other on the die and are connected by the large routing channel which dominates the center of the die area. These common inputs and outputs are then routed to the edge of the die where they are bonded out to the package.

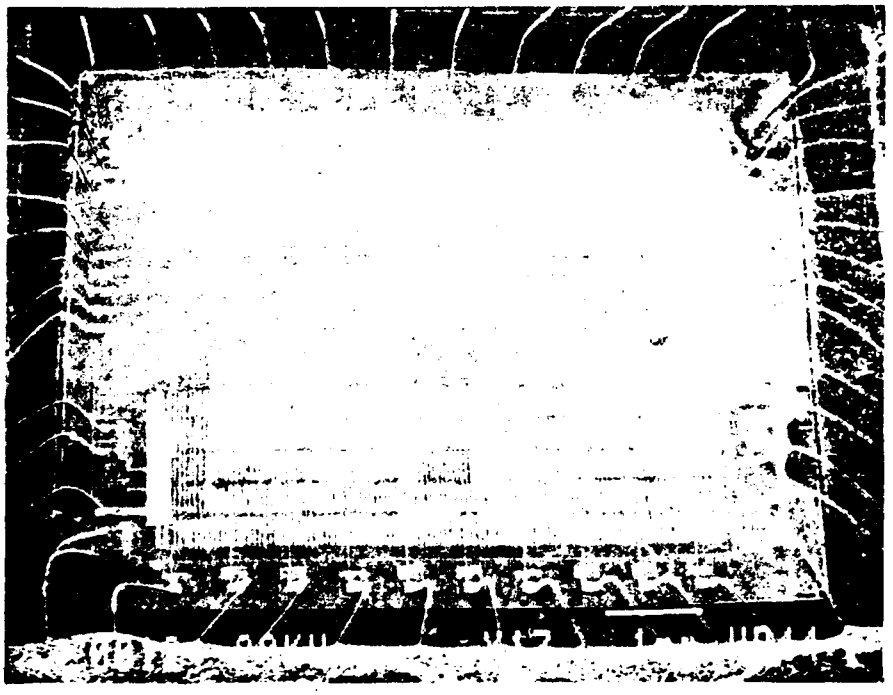


Figure 46 Test Vehicle SEM Photograph

5.2 Input/Output Cells

The input and output cells used in the design of the test vehicle are standard CMOS I/O cells. The schematic of the output driver is shown in figure 47 and a SEM photograph of the output driver is shown in figure 48. It is a simple design which uses multiple inverter stages to fan up to a very large output stage. Minor modifications are made to the relative transistor sizes in the next to last drive stage to ensure that either output transistor turns off slightly before its complement turns on. This drastically reduces the switching current of the output driver.

The schematic of the input receiver is shown in figure 49 and a SEM photograph of the input receiver is shown in figure 50. The receiver is also a fairly simple design since it again uses multiple inverter stages to fan up to a driver circuit capable of driving signals which may traverse the entire die. The receiver design is complicated somewhat by an electrostatic discharge (ESD) protection network which consists of a series input resistor, two diodes to VSS, and a distributed diode to VDD.

The design is also complicated by a small pull up transistor which both provides compatibility with TTL driver as well as preventing an undriven input pad from floating to 1/2 VDD and consuming large amounts of power. Although this pull up device is normally a prudent design technique, it proved to be a nuisance on this project.

The life test boards drive up to 24 test vehicles in parallel as is detailed in the schematics in appendix D. Since some inputs are shared between test vehicle halves, this means that the level converters on the lifetest board must be able to drive 48 input receivers. The small pull up transistor in each receiver sources 5 mA of current which makes this task extremely difficult. In addition, one of the periodic tests we performed in order to find any gate oxide failures was a measurement of static ICC at each test vector in the functional test pattern. Any ICC variation due to a gate oxide short is difficult to remove from the large background ICC due to the pull up transistors. Figure 51 is a plot of a portion of the ICC measurements taken at initial electrical characterization.

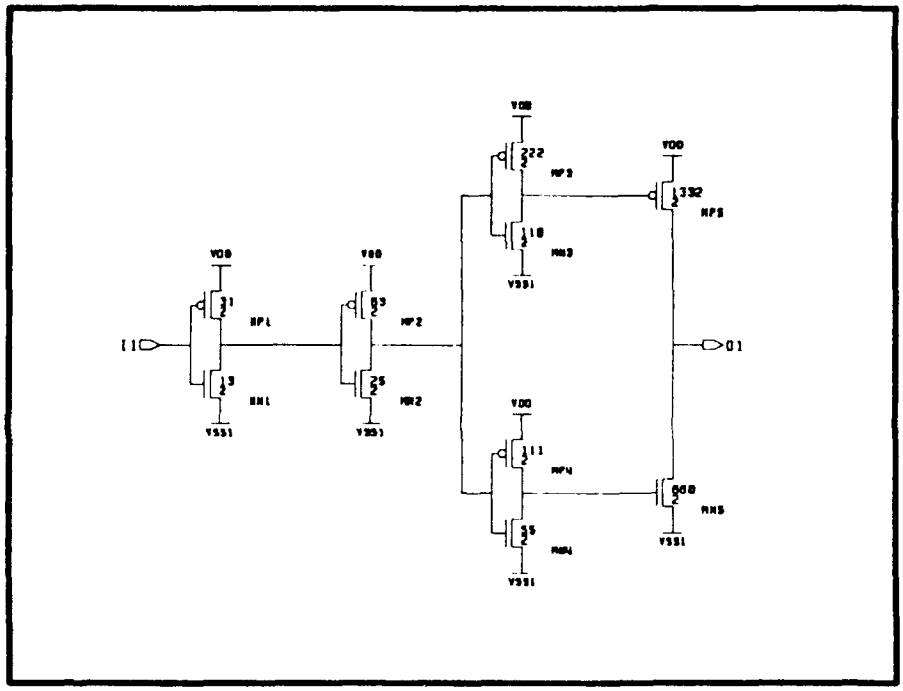


Figure 47 Output Pad Schematic

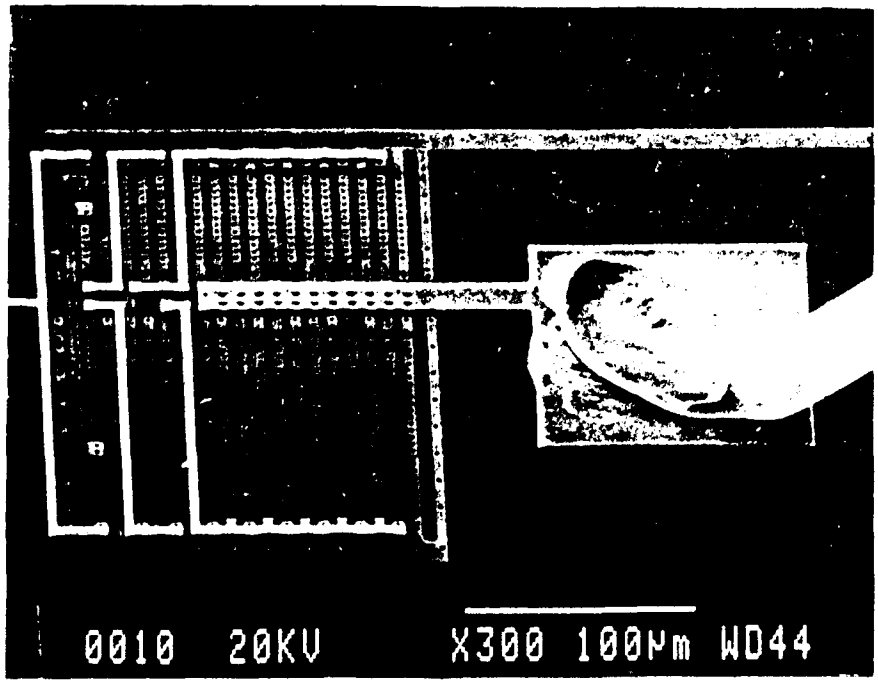


Figure 48 Output Pad SEM Photograph

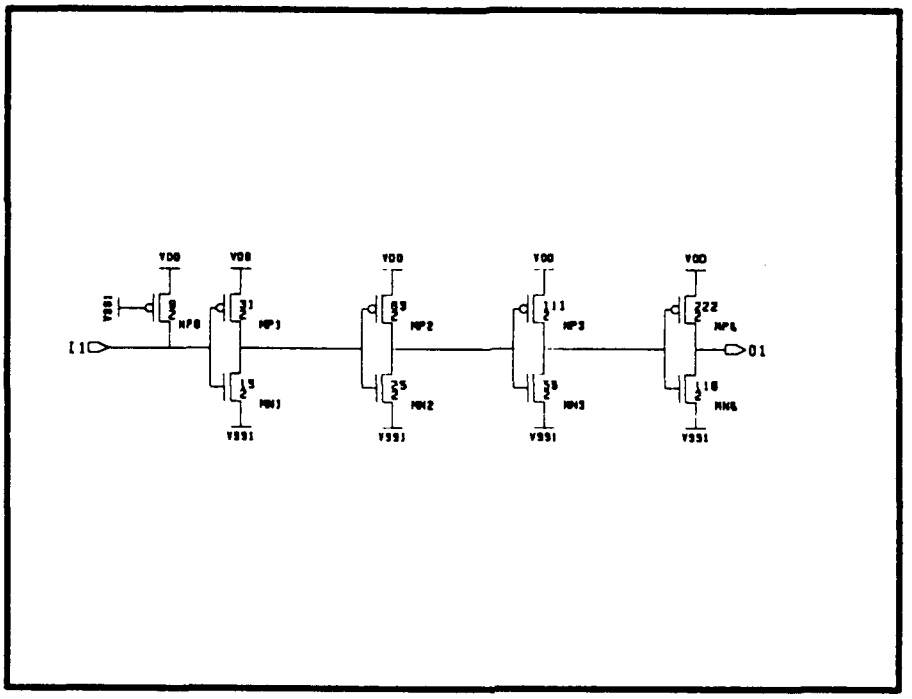


Figure 49 Input Pad Schematic

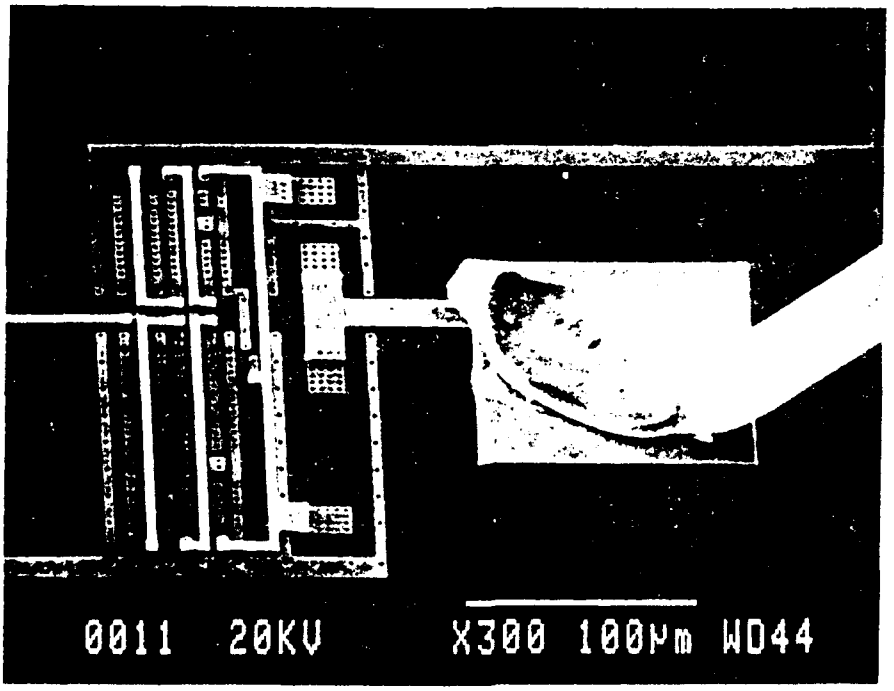


Figure 50 Input Pad SEM Photograph

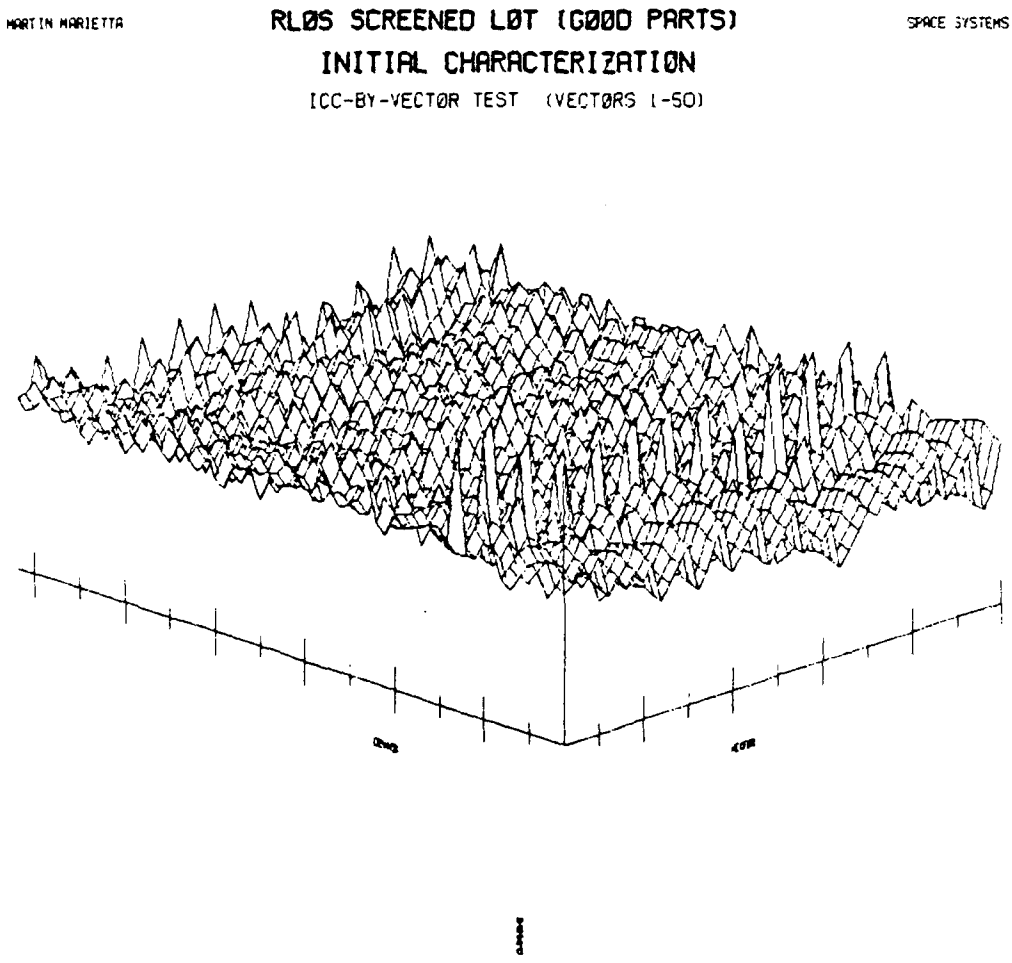


Figure 51 Partial Initial ICC Measurements

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

5.3 Internal Screening Circuitry

The operation of the internal screening circuitry incorporated in Test Vehicle B is described in section 3. This section describes details of the physical implementation. Figure 52 shows the schematic of decoupling/stress circuit used throughout Test Vehicle B. It consists of four transistors (QA, QB, QC, and QD) which are controlled by four separate signals (SA, SB, SC, and SD). The physical layout of this circuit is shown in figure 53.

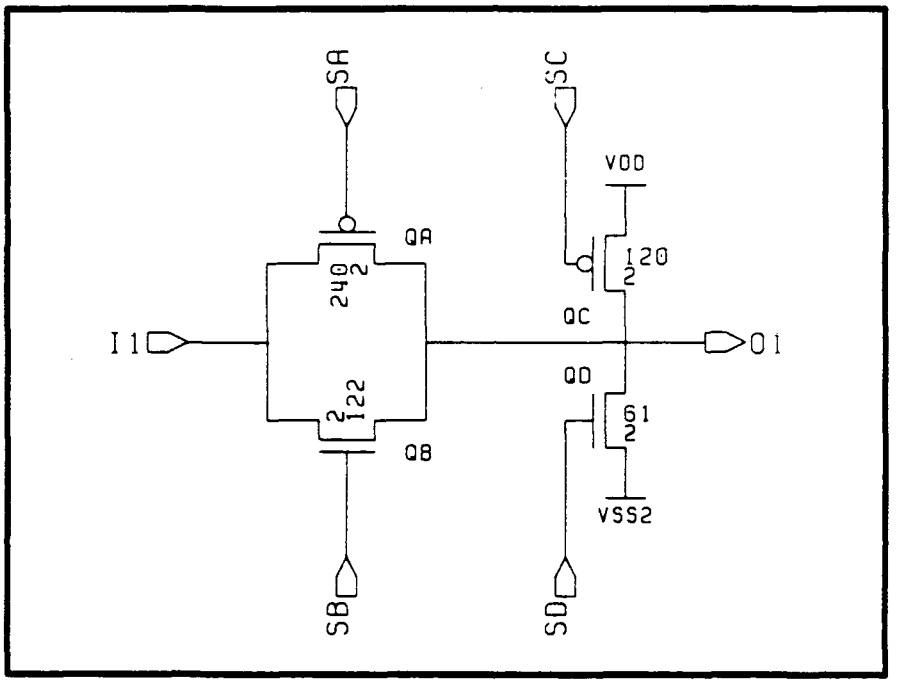


Figure 52 Decoupling/Stress Circuitry Schematic

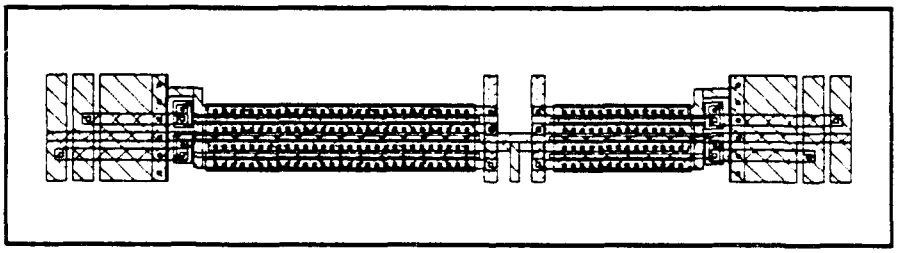


Figure 53 Decoupling/Stress Circuitry Physical Layout

The use of this screening circuitry does have drawbacks as detailed in figure 54. This figure displays a 2 input NAND gate without the screening circuitry on the left and the same gate with the screening circuitry incorporated on the right. As shown in the figure, use of this screening circuitry results in about a 70% increase in cell area and a 100% increase in

propagation delay. Finally figure 55 is a SEM photograph of a portion of a standard cell row in Test Vehicle B which includes the internal screening circuitry.

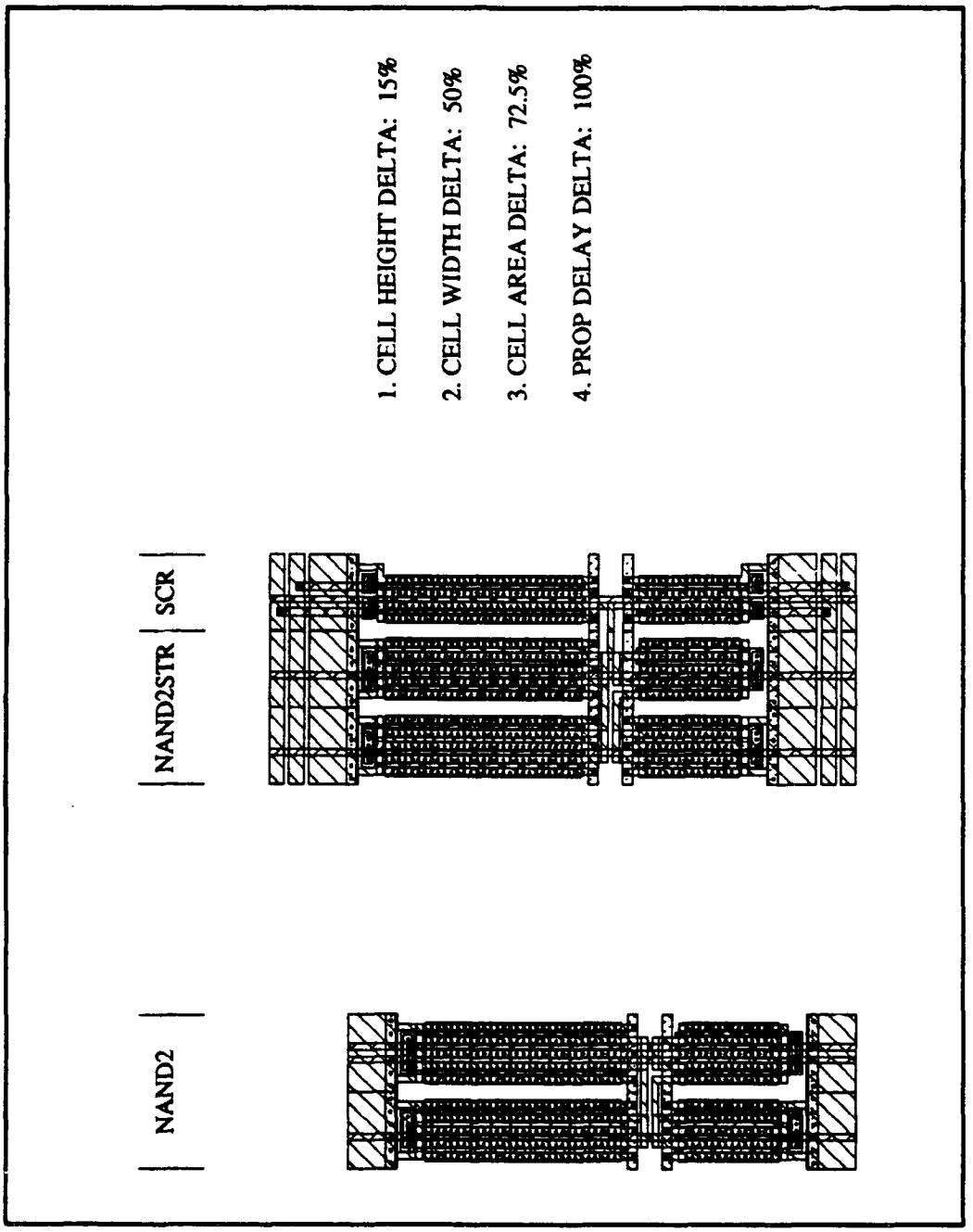


Figure 54 Screen Circuitry: Cell Area and Speed Penalties

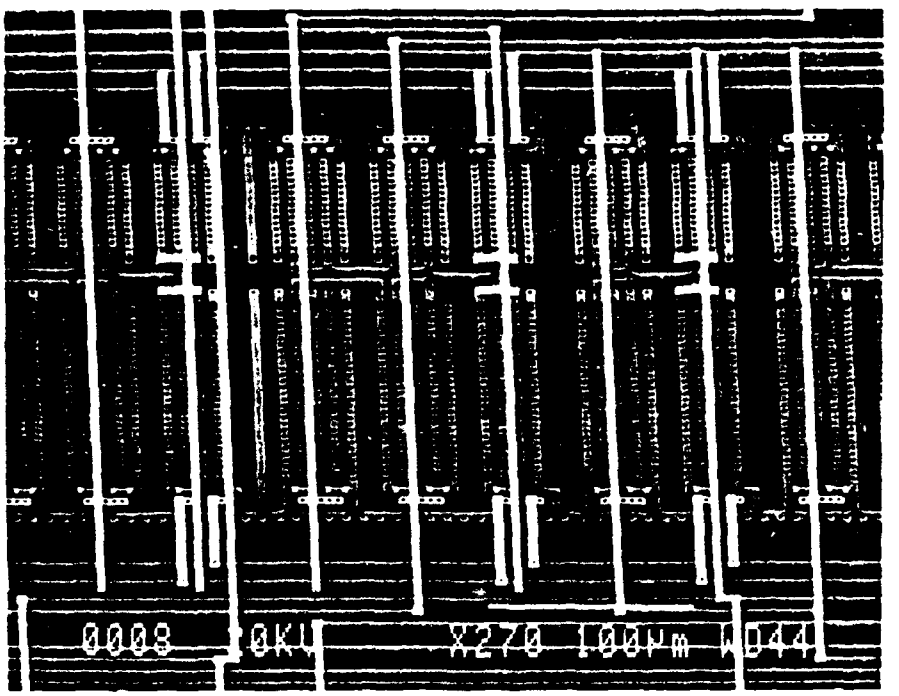


Figure 55 Screen Circuitry: Cell Row SEM Photograph

The internal screening circuitry uses four independent signals (SA, SB, SC, and SD) to control the decoupling/stress elements throughout the device. However, we decided not to have four independent input pins which correspond to these four control signals. Instead we designed Test Vehicle B to have two stress control input pins (S1 and S0) which are decoded to provide the four internal stress control signals. The first reason for this is that there were not enough pins available on the package to support all four stress inputs without further reducing the complexity of the MSI circuitry in the test vehicles.

More important however is that we decided it was too risky to have all four stress signals directly controllable at the input pins since this would allow the user to accidentally short VDD to VSS by incorrectly controlling the stress inputs. It was decided that a more prudent approach would be to provide internal decoding circuitry which prevents a VDD to VSS short regardless of the state of the stress input pins. It was recognized that this approach would somewhat degrade the ability to achieve even stress but the approach of having all four stress controls accessible was deemed too risky.

Figure 56 is a schematic diagram of this stress decode circuitry. Figure 57 is the physical implementation of this design. Finally, Figure 58 is a SEM photograph of the stress decode circuitry as implemented on Test Vehicle B.

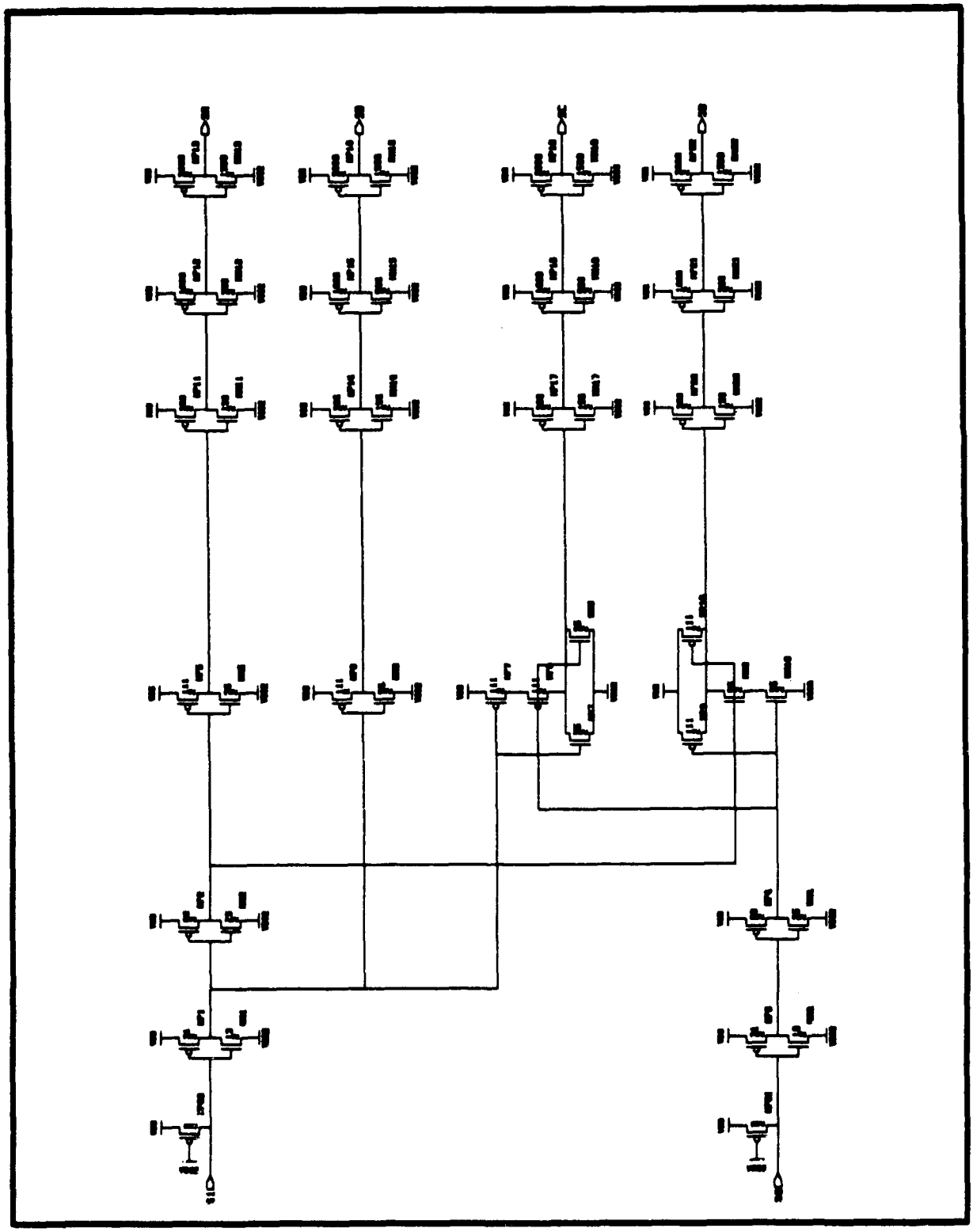


Figure 56 Stress Decode Circuit Schematic

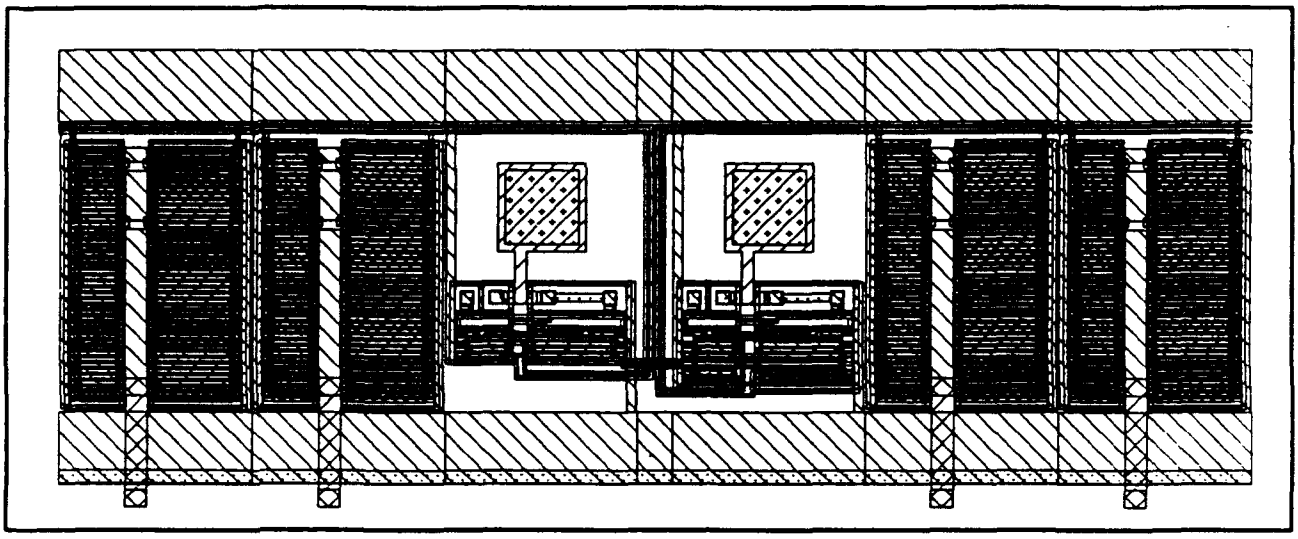


Figure 57 Stress Decode Circuit Physical Layout

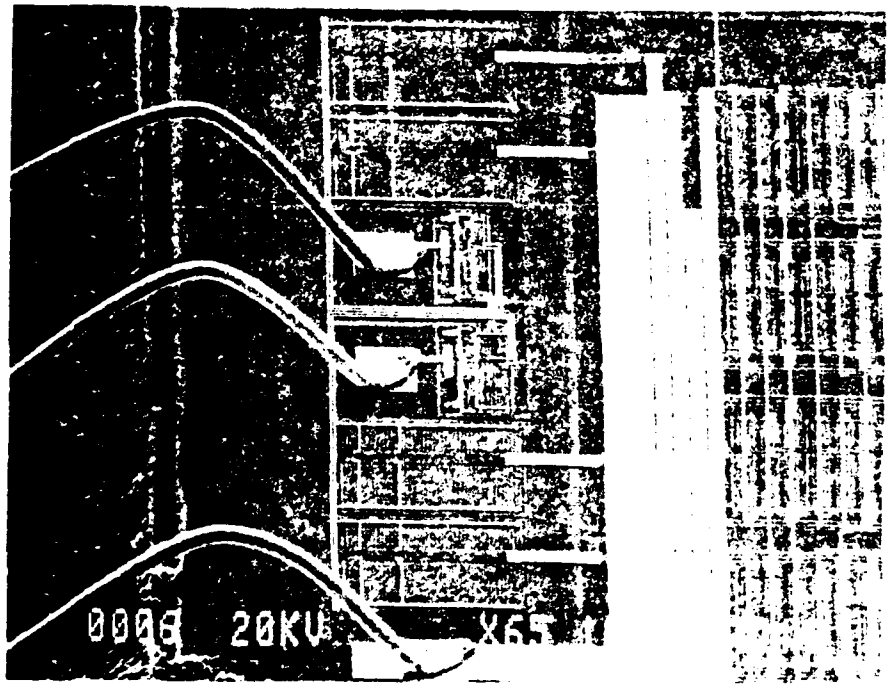


Figure 58 Stress Decode Circuit SEM Photograph

5.4 Stress Histograms and Oxide Defect Predictions

Both test vehicles were simulated in order to develop an optimum test vector set for use during electrical screening as well as a test vector set for use during the life test. Figure 59 shows stress histograms for both an initial and a final optimized test vector set for Test Vehicle C. For the final test vector set the stress duty cycle for TVC has a mean of 48% and a standard deviation of 27%. Figure 60 likewise shows initial and final stress histograms for Test Vehicle B which contains the internal screening circuitry. In this case both histograms reflect the usage of the internal screening circuitry but use the same functional test vectors as used for Test Vehicle C. The final histogram for Test Vehicle B has a stress duty cycle with a mean of 45% and a standard deviation of 19%. Note that all of these histograms have a range of .95, or a ratio of 50 to 1 between most and least stressed.

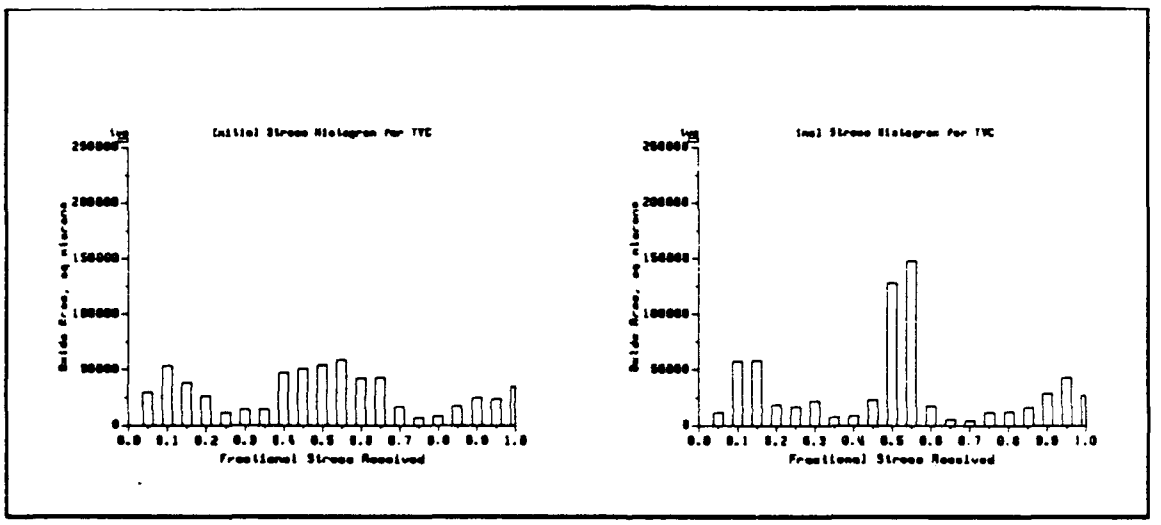


Figure 59 Stress Histograms for Test Vehicle C

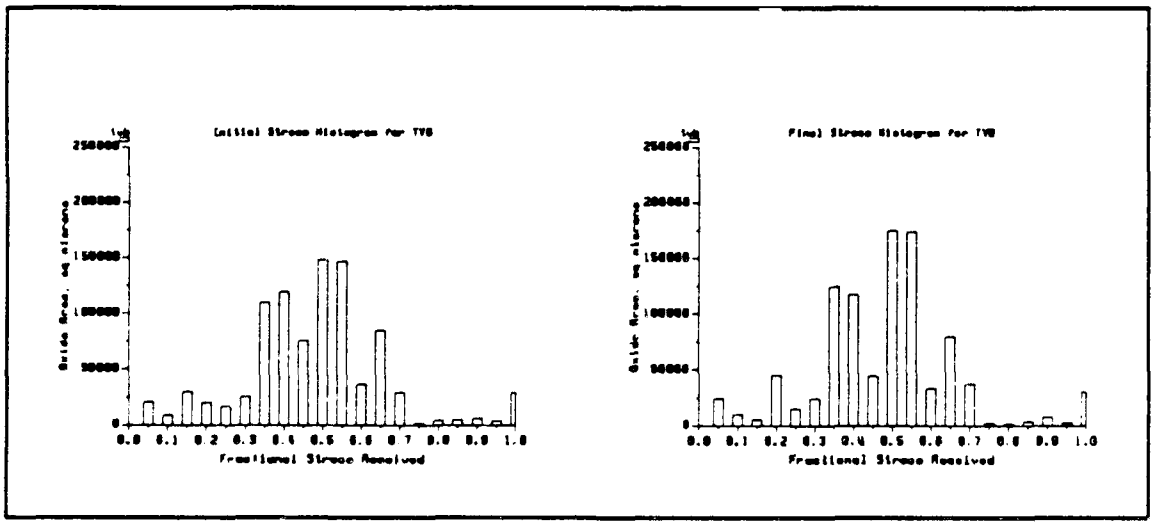


Figure 60 Stress Histograms for Test Vehicle B

In addition we have performed simulations on Test Vehicle B assuming that all four stress control signals are available at the chip inputs. This gives an indication of the extent to which the stress decode circuitry interferes with evenly stressing the gate oxide on the chip. Figure 61 shows the stress histogram for the case where SA, SB, SC, and SD are all available at the chip inputs. The histogram for Test Vehicle B in this special case has a stress duty cycle with a mean of 47% and a standard deviation of 17%. Of equal importance, it should be noted that the absolute range of stress duty cycles received in this special case is only 0.75 compared with 0.95 for the normal simulations of both test vehicles.

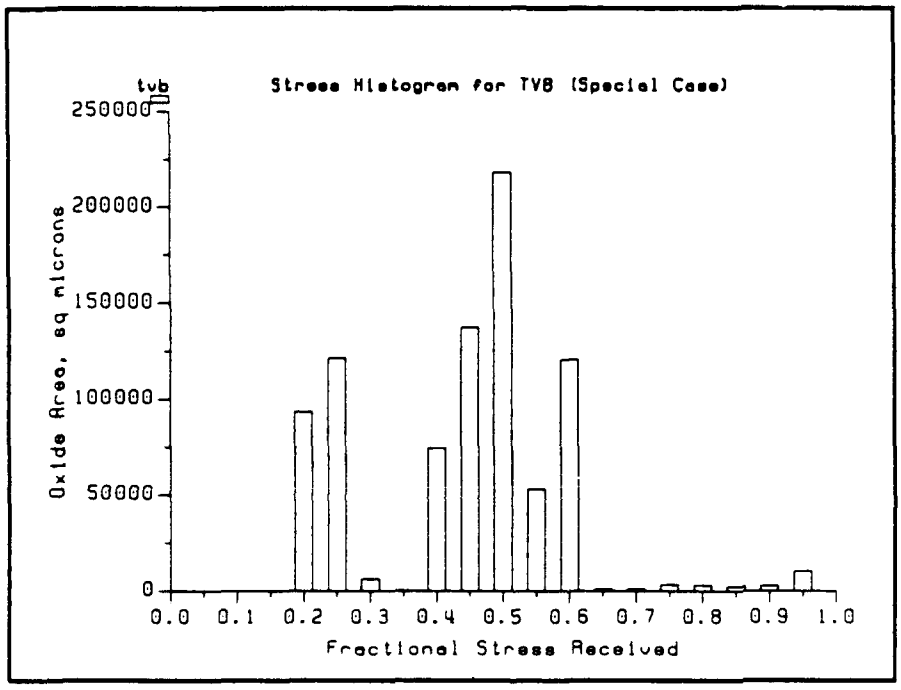


Figure 61 Stress Histogram for Special Case Test Vehicle B

Data presented in section 2 indicated a defect density of about three defects per square centimeter for a gate oxide similar to that used in fabricating the test vehicles. The total oxide area of Test Vehicle C is 6.2E-3 square centimeters which yields an expected 3 oxide defects in our lot of 150 parts. The total oxide area of Test Vehicle B is 9.2E-3 square centimeters which yields an expected 4 oxide defects. However it is expected that these defects would be found with a simple 5V functional test and thus would have been screened out at the foundry prior to packaging. It must be noted that these calculations are based on gate oxide test structures fabricated at a different foundry than the test vehicles. The actual gate oxide defect density figures for the test vehicles are not known. The numbers given above serve only as a rough estimate of the number of defects which may be present in a lot of 150 parts.

6. Life/Screen Test Board Design

At project inception it was not known whether a screen could be developed which would be of short enough duration to be performed on the test head of the automated test equipment (ATE). If a short duration screen on the test head produced no results, it would be necessary to attempt a longer duration screen with the test vehicles in-situ in the life test board. In order to accomplish this we designed a fairly flexible board which could be configured to handle the requirements of either screen or life test. A top level functional block diagram of a test board is shown in figure 62 while detailed schematics can be found in appendix D.

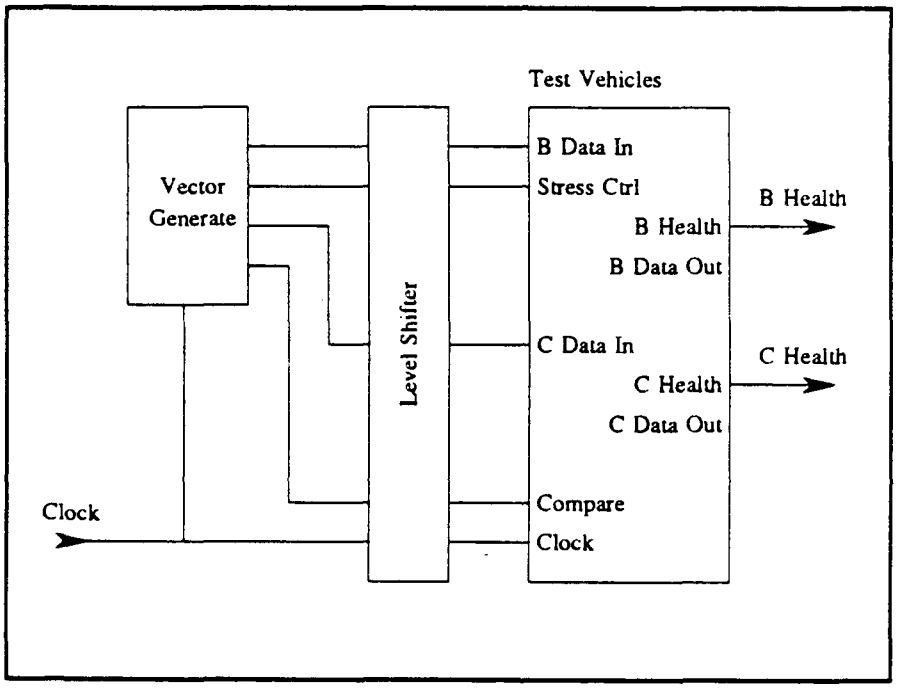


Figure 62 Life Test Board Functional Block Diagram

Figure 63 shows the circuitry which generates test vectors for the test vehicles. Three 4-bit synchronous counters are chained together to form a 12-bit counter. This 12-bit counter forms the address field for three UV erasable EPROMS which together form a 24-bit vector field. Twenty two of these bits are used to dynamically exercise the test vehicles. In addition one bit is used to reset the address generation counters at the end of the test vector set. In this way nothing in the hardware except the depth of the EPROMS controls the length of the vector set.

The clock input was supplied by a fixed, on board, 250KHz clock generator. This fixture originally was to be used only for life tests. When it became apparent that the devices would have to be screened at high voltage for a longer time, a board was modified to allow screening at 1KHz. Ideally, screening should take place at the lowest possible frequency, perhaps even with Vdd lowered to 5v or less during clock transitions, to reduce the magnitude of switching transients. This is especially true of test vehicle B because so many transistors switch at the same time during the screening vectors.

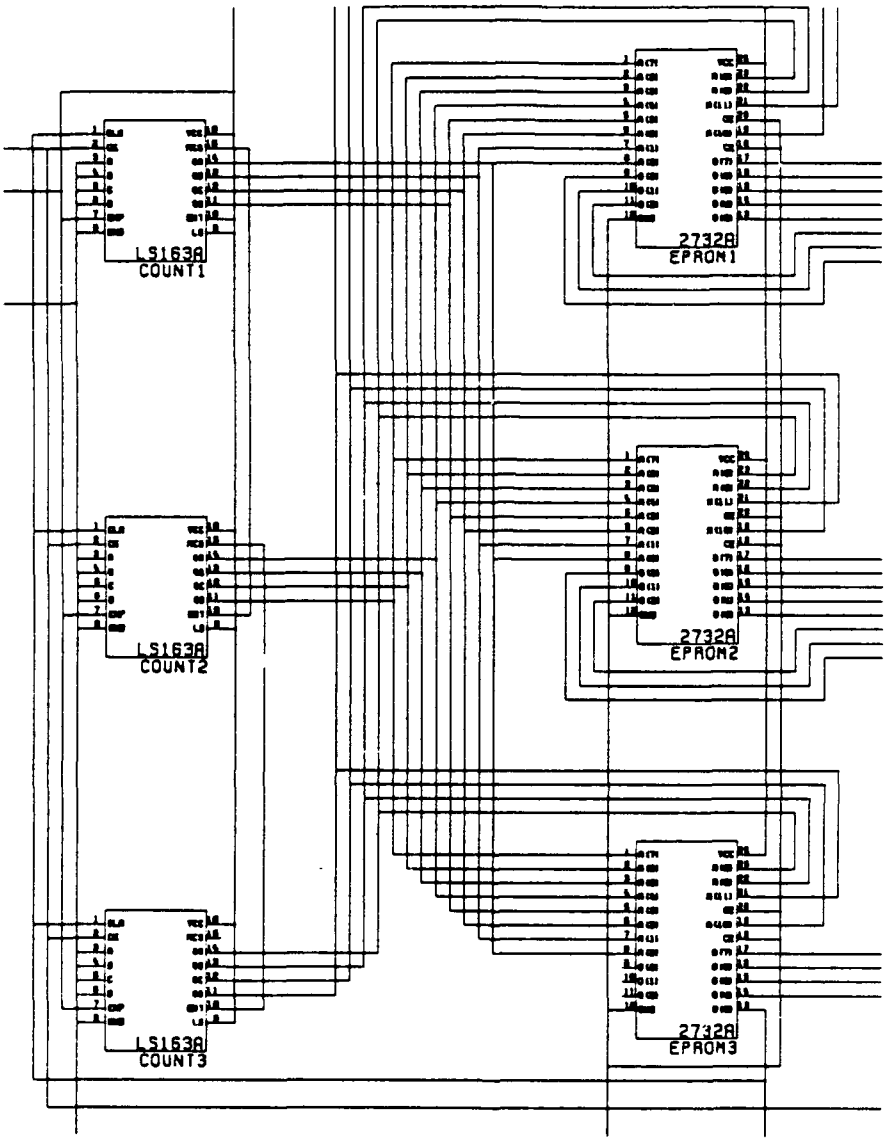


Figure 63 Life Test Board Test Vector Generation

Since all the inputs to the test vehicles need to be at a higher voltage in order to induce stress, a level shifter is included in the test board. This level shifter is designed to convert TTL level signals to CMOS levels. It has an independent power supply pin which determines what voltage the CMOS parts are using. This level shifting circuitry is shown in figure 64.

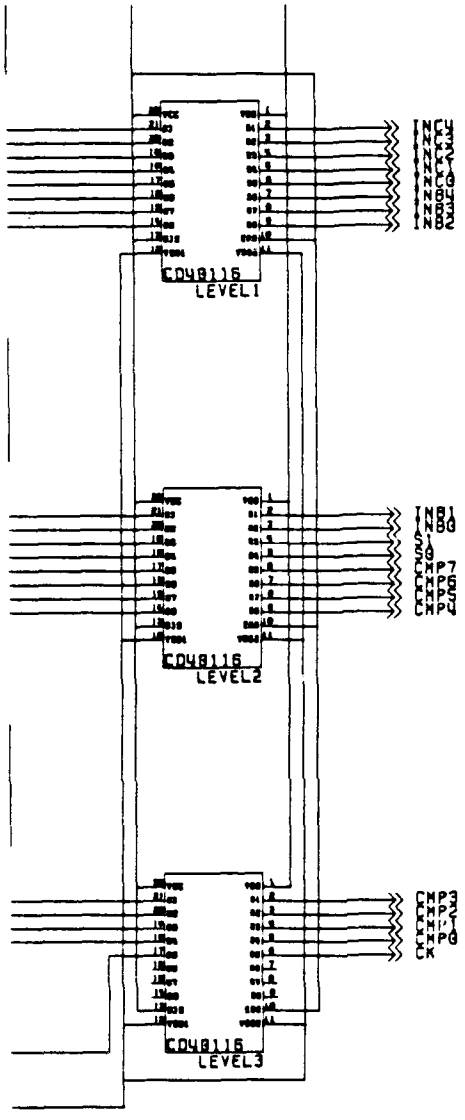


Figure 64 Life Test Board Level Shifting

During the life test the data inputs of the two test vehicles are identical. However during the screen the two test vehicles receive different data inputs. This necessitates separate busses to control the data inputs of the two test vehicles. In addition Test Vehicle B requires two inputs to control the internal screening circuitry. However, the compare and clock inputs are identical for both test vehicles so only one bus is needed for this function.

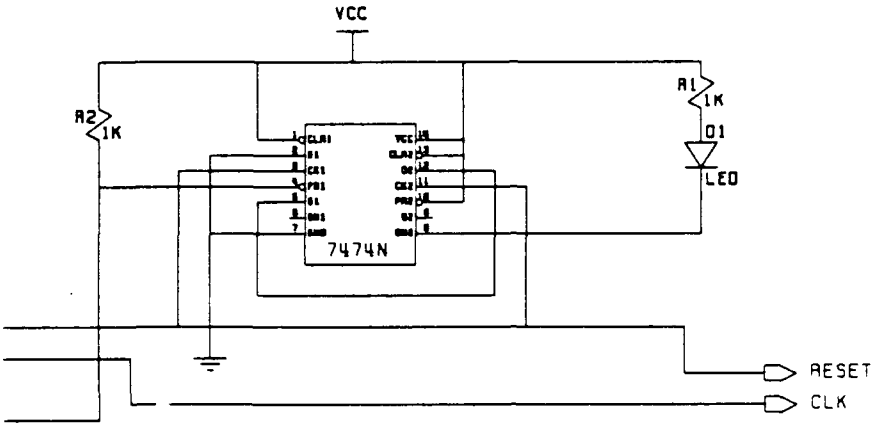


Figure 65 Life Test Board Master Health Monitor

Each test vehicle contains three health monitors: one for each half of the test vehicle (OKB and OKC) and a combined open drain health monitor (OK). The open drain health monitors are wired together to form one master health monitor for each board. This master health monitor, along with some peripheral circuitry, drive an LED which is used to visually monitor the status of the entire board. This master health monitor circuitry is shown in figure 65. Finally, all of the individual health monitors as well as the master health monitor and the clock are available via a 50-pin connector for use in checking the status of individual test vehicles on the board.

7. Electrical Screening

7.1 Test Pattern Development

The first task in the electrical screening portion of this program was to develop test vector sets to be used on the test vehicles during both the screen and life test. During the screen the two test vehicles received different test vector sets. Test Vehicle C was exercised using a test vector set which has been optimized to provide as even oxide stress as possible. Test Vehicle B which contains the internal screening circuitry was exercised using a different test vector set which takes full advantage of this additional circuitry. During the life test on the other hand, both test vehicles were exercised using the test vector set developed for screening Test Vehicle C.

Thus only two vector sets needed to be developed. The process used in this development was a mixture of computer aided and manual analysis of various test vector sets. This is illustrated in figure 66.

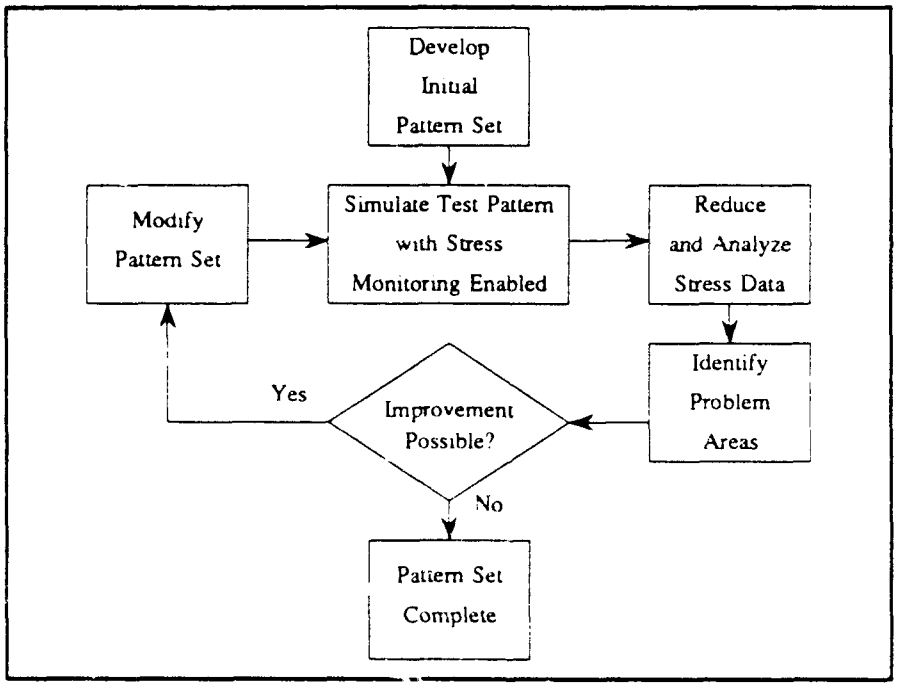


Figure 66 Test Pattern Development Flow Diagram

We began with initial test vector sets which we believed would stress the gate oxides in the test vehicles fairly evenly. Then we simulated the test vehicles when exercised with these test vector sets on our CAE workstations and used the test pattern evaluation portion of the Oxide Stress Analyzer (OSA) software to evaluate the test pattern sets and identify oxide areas in the test vehicles whose stress duty cycles were furthest from the mean. Most importantly, we used this software to identify any oxide areas which were not stressed at all

We then utilized manual methods to modify the test vector sets to improve the evenness of the oxide stress coverage. This cycle was repeated until we decided that no further improvements in the stress coverage of the test vector sets was practical. Stress histograms for the final test vector sets developed were presented in section 5.4 and complete listings of the test vector sets are presented in appendix E.

7.2 Failure Rate Calculations

Once the test vector sets were developed, the stress coverage characteristics of the vector sets were to be combined with the oxide characterization database presented in section 2 in order to predict failure rates for the test vehicles. The technique we were to use is illustrated in figure 67.

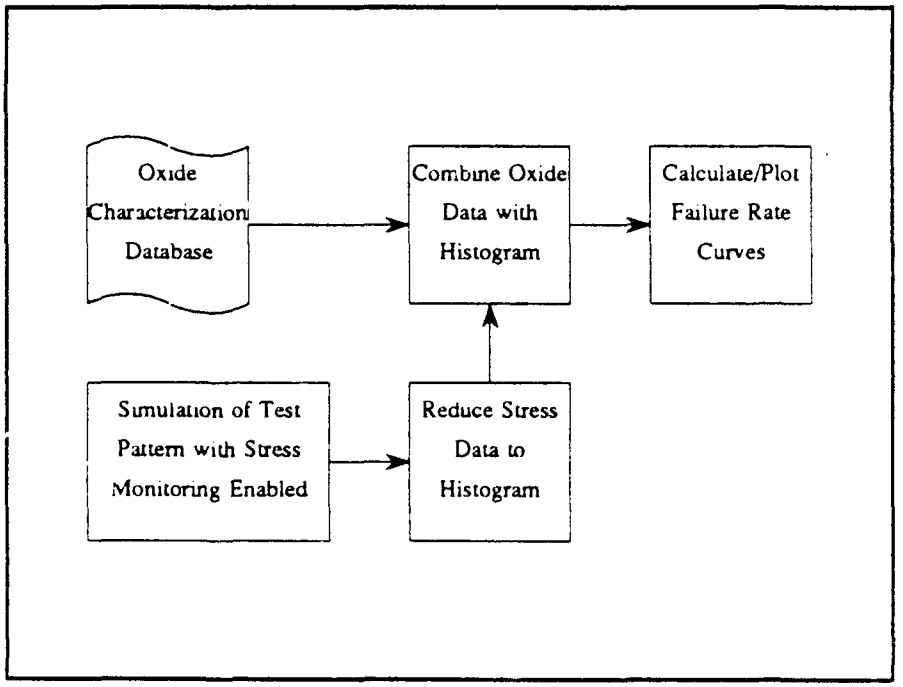


Figure 67 Failure Rate Calculation Flow Diagram

To begin, the test vehicle is broken into a number of portions receiving roughly equal stress duty cycles. Next the total oxide area of each of these test vehicle portions is calculated. This so far is simply the information needed to generate any of the stress histograms presented earlier.

The results of characterizing the gate oxide can then be used to calculate failure rate curves for each bin of the stress histogram by correcting for area and the stress duty cycle of that bin. Finally, a failure rate curve for the entire device may then be calculated by simply adding together the failure rate curves for each bin.

Unfortunately, we were unable to perform these calculations. Since we were not able to characterize the gate oxide with a fixed field stress we had no data available to perform failure rate versus time calculations. The best we could do is to generate the failure rate as a function of E-field curves for the test vehicles that were presented in section 2.6, Figures 30 and 31, pg. 39.

7.3 Prescreen

The purpose of the prescreen was to verify that the parameters chosen for the final screen yield the desired screening effect during the life test. The prescreen was performed on 50 parts and was to last up to 500 hours based on the failure rates observed. To allow a screen of this duration to occur, the prescreen had to be performed with the test vehicles inserted into the life test boards and with the EPROMS programmed with the screen vector set.

Discussions with the test vehicle vendor indicated that one of the wafers fabricated had a source/drain to p-well junction breakdown voltage of 9.5 V. Testing on some of our sample devices indicated that this was true and that a stress voltage of 12 V as originally planned would not be possible. Thus the decision was made to use a stress voltage of 9 V during the prescreen. However, since the oxide thickness of the test vehicles is in the 225 Angstrom range, this yielded a respectable E-field of 4 MV/cm.

When the test vehicles were checked 48 hours into the prescreen (during a screen the health monitor circuitry is non-functional and thus dynamic monitoring was not possible) it was found that many of the test vehicles failed functionally and exhibited extremely high ICC. A visual examination of several of these failed parts revealed burn marks on the large n-channel transistor which drives the stress control pullup p-channel transistors. As a result these p-channel pullup transistors were presumably turned on all the time which resulted in the extremely high ICC measurements.

At this point we evaluated the integrity of the electrical signals on the life test boards during the screen program. Although the boards performed perfectly while the life test program was loaded into the EPROMS, we found very large transient currents and voltage ringing on the board when the EPROMS were programmed with the screen test vector set. This was due to the internal stress control circuitry on Test Vehicle B.

When the stress control circuitry is enabled in either the pull high or pull low mode, every signal node in Test Vehicle B is pulled high or low simultaneously. This dumps a very large amount of current on either the VDD or VSS rail. At the operating frequency of the test boards (250 kHz) this generated a tremendous amount of noise. As a result the stress received by the test vehicles was not at all well controlled. In addition the test vector generation portion of the test boards did not even operate dependably under these conditions.

Due to these problems with performing a screen with the test vehicles in-situ in the test boards it was decided that the best screen we could attempt was a short, controlled, 9 V screen performed on our S-3260 tester.

7.4 Screen

The screen test vector set was then ported to the S-3260 tester and a small screen test program was developed. This program simply looped through the screen vector set at 9 V for 5 seconds. We performed this screen on the appropriate lot of 150 parts. No parts failed this screen. It was then decided that since the success of the entire program rested on performing a successful screen, we had to make another attempt at a longer duration screen using the test boards.

To accomplish this we modified one test board by cutting the trace from the on-board 250 kHz clock oscillator and directly driving the board's clock via a benchtop signal generator at 1 kHz. Initial tests and monitoring throughout the screen indicated that the test boards were capable of applying a clean screen test vector set at this frequency. We then began a two hour screen with the parts going on to the modified board in lots of 20.

During the screen the modified test board developed a short between two of it's signal traces. Due to the inability to perform dynamic health monitoring during the screen, 40 test vehicles were destroyed due to this board level short before the problem was detected. We isolated the short and decided to simply scrap that board and modify another one to use for the remainder of the screen.

We completed the two hour in-situ screen on 150 parts. No parts failed functional test following this screen except for the 40 parts destroyed by the board short. However we did observe a fourfold increase in average ICC following the screen. Since the integrity of the signals reaching the test vehicles were monitored during the screen, it was decided that the 9 V stress was too much for the devices to withstand.

We therefore decided to reduce the voltage to 8 V for the accelerated life test. However it was realized at this point that the screened parts could be seriously weakened due to the 9 V stress and that this could effect the results of the accelerated life test.

8. Accelerated Life Testing

The accelerated life test lasted 4000 hours and was performed at room temperature with a stress voltage of 8 V. Early in the life test our dynamic monitoring revealed a single event which resulted in 18 parts failing. Failure analysis on several of the failed parts revealed that the VSS2 bond wire was fused open.

It was discovered that the life test boards were inadvertently powered from an unconditioned power outlet. We believe that the blown VSS2 bond wires were the result of an abrupt power up after a building power failure. To remedy the situation we moved the life test setup so that it was powered via the main lab power conditioner. We also modified the power conditioner reset procedure to include turning off power to the test boards before restoring lab power.

The electrical characterization following the first 1000 hour segment of the life test showed that many more parts were damaged during the screen and at the beginning of the life test than initially realized. A large number of parts (both screened and unscreened) displayed a greatly exaggerated ICC. This is consistent with damage sustained via a supply voltage overstress. The overstress damaged the source/drain to p-well junction diodes of the n-channel transistors. This damage while not detectable immediately on some lesser damaged devices eventually shows up as high leakage through these diodes and thus high ICC measurements. Figure 68 displays the initial ICC measurements from the screened lot. Contrast this with figure 69 which displays the same ICC measurements after the first 1000 hour life test segment. To put things in perspective, note that the interim data is displayed at 1/10th the magnification of the initial data. Thus the peaks in figure 69 are indeed very high.

The remainder of the life test was uneventful. Throughout the duration of the life test more parts dropped out remaining functional but displaying high ICC. Detailed plots of the electrical characterization data taken throughout the life test are shown in appendices F and G. In addition, details of the failure analyses performed on failed parts are presented in section 9.

The plots were intended to be used to easily identify parts immediately as they began to display anomalous behavior. However, due to the large number of gross device failures and due to the steady increase in ICC throughout the lifetest, these plots were of little use. Therefore, to analyze the lifetest data and categorize the failures, we resorted to a detailed manual inspection of all the raw electrical characterization data.

In retrospect, it would have been more useful to measure static ISS as a function of test vector rather than the ICC measurements that we performed. This is because the leakage current due to the pullup transistors in the input pads does not show up in an ISS measurement. We therefore also performed this ISS measurement for the final electrical characterization. The results of this are also displayed in appendix G. In the final analysis, the ISS measurements also proved unrevealing due to the large number of devices displaying high current. Even in the ISS measurements, any current due to a gate oxide short is overwhelmed in the drastically increased junction leakage current.

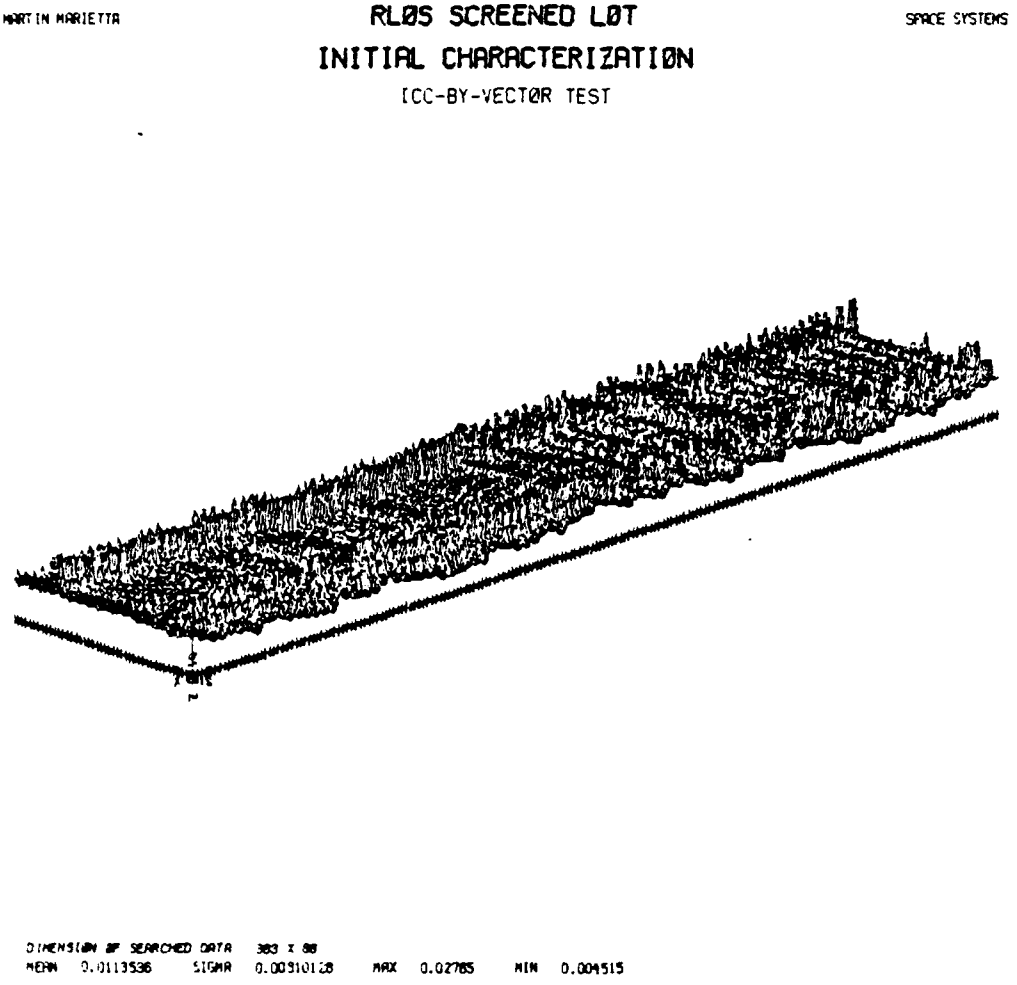


Figure 68 Initial ICC Measurements

X-Axis: Vectors 1-383
Y-Axis: Devices 1-88
Z-Axis: ICC 0-30mA

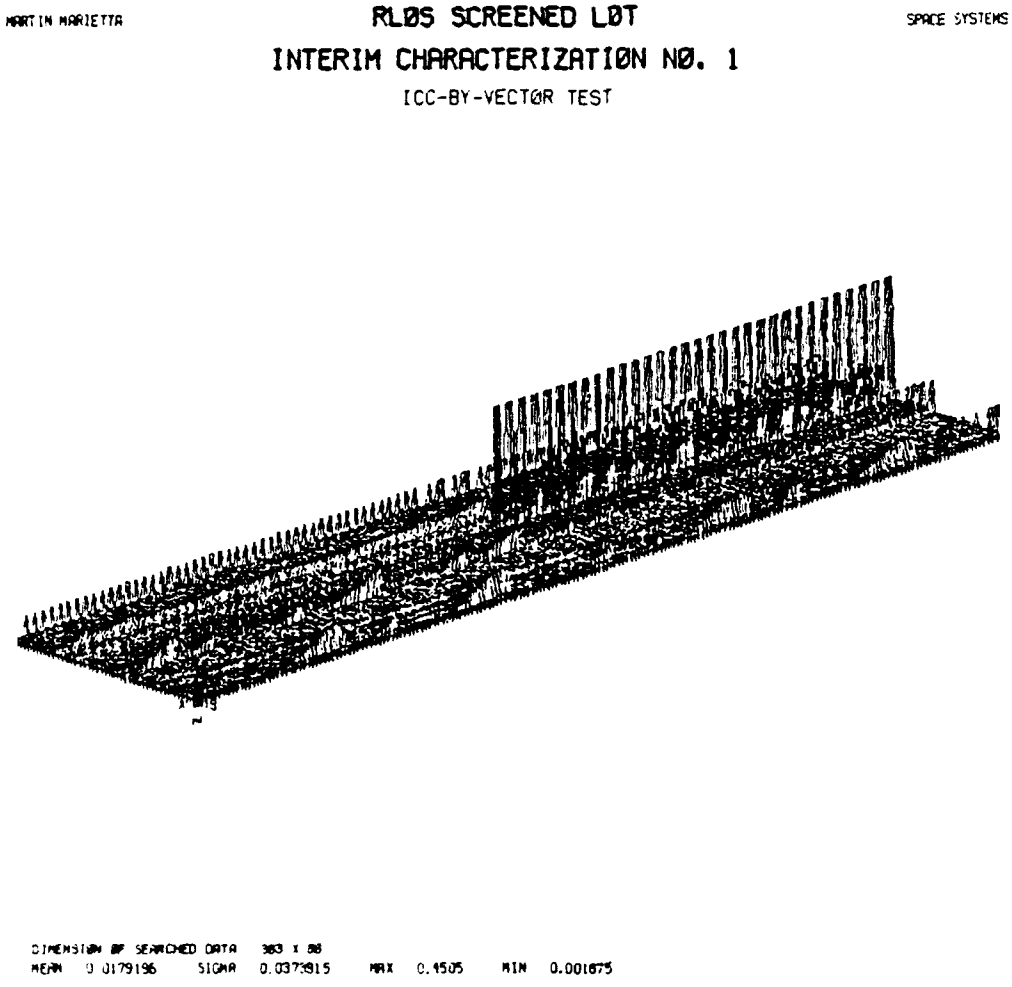


Figure 69 1000 Hour Interim ICC Measurements (1/10th Scale)

X-Axis: Vectors 1-383
Y-Axis: Devices 1-88
Z-Axis: ICC 0-500mA

9. Failure Analysis

9.1 Failed Parts Data Summary/Analysis

During the course of the 4000 hour life test 107 parts were declared failures. These failed parts displayed a variety of electrical characteristics from functional test failure to abnormally high measured ICC. Full electrical characterization was performed following the life test in order to determine which failures, if any, were due to oxide breakdown. Due to the large number of failures, it was decided that if a failure could be attributed to input / output pad voltage overstress, that part would not undergo further failure analysis. Following is a data summary and analysis of the failed parts. Only a few devices displayed failed electrical characteristics which could not be attributed to I/O pad damage. A few parts, representative of these non pad related failure modes were then subjected to destructive physical analysis. The results of this are detailed in section 9.

```
#
# ANALYSIS OF FINAL ELECTRICAL CHARACTERIZATION
# ON ALL FAILED RLOSTV DEVICES BY SERIAL NUMBER
#

-----------------------------------------------------------------------
SN001:
  Functional:      No functional failures.
  ICC:             High ICC (8X) corresponding to pin S1 low (no stress).
  Input Current:   IIH (2X) for all pins, IIL nominal.
  Output Current:  IOH nominal. IOL nominal for TVC, high (20X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH nominal, VOL nominal for TVC, high (2X) for TVB.
  PROGNOSIS:       I/O damage.  Probable damage to stress control.
-----------------------------------------------------------------------
SN002:
  Functional:      No functional failures.
  ICC:             High ICC (2X) corresponding to pin OKB high.
  Input Current:   IIH (2X) for all pins, IIL nominal.
  Output Current:  IOH nominal. IOL nominal for TVC, high (20X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH nominal except for 4.5V on OKB.  VOL nominal
                   for TVC, high (2X) for TVB.
  PROGNOSIS:       I/O damage
-----------------------------------------------------------------------
SN006:
  Functional:      Failed pins: OK, OKB, OUTB(0,4,5,8).
  ICC:             High ICC (10X) corresponding to pin S1 low (no stress).
  Input Current:   IIH (2X) for TVC, (3X) for TVB, IIL nominal.
```

```
  Output Current: IOH nominal. IOL nominal for TVC, high (30X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, high (3X) for TVB.
  PROGNOSIS:      I/O damage.  Probable damage to stress control.
-------------------------------------------------------------------------
SN010:
  Functional:     No functional failures.
  ICC:            High ICC (2X) corresponds to S1 high and S0 low.
  Input Current:  Nominal.
  Output Current: IOL nominal. IOH (2X) for OUTB(1), OKB, OKC.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable stress control damage.
-------------------------------------------------------------------------
SN011:
  Functional:     No functional failures.
  ICC:            High ICC (2X).  No obvious correlation with any pin.
  Input Current:  Nominal.
  Output Current: IOH nominal. IOL high (2X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN020:
  Functional:     No functional failures.
  ICC:            High ICC (2X). May correspond with OKB high.
  Input Current:  Nominal.
  Output Current: IOH nominal. IOL nominal for TVC, (2X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN056:
  Functional:     Failed pin: OUTB(7).
  ICC:            High ICC (20X) corresponding to OKB high.
  Input Current:  IIH (3X) for INB(3) and S0. IIL (4X) for CMP(0).
  Output Current: IOH nominal, IOL high (20X) for many pins.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Many out of spec.  OUTB(7) VOH = 0.5V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN059:
```

```
  Functional:     Failed pin: OUTB(6).
  ICC:            High ICC (10X) corresponding to OUTB(6) high.
  Input Current:  Nominal.
  Output Current: Nominal.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal except OUTB(6) VOH = 0.5V
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN066:
  Functional:     Failed pin: OUTB(7).
  ICC:            High ICC (10X) corresponding to OUTB(7) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, high (2X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal except OUTB(7) VOH = 0.5V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN071:
  Functional:     Failed pin:  OUTB(2).
  ICC:            High ICC (2X) corresponds with OUTB(2) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, high (5X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal except OUTB(2) N-channel test = 0.03V.
  Output Voltage: Nominal except OUTB(2) VOH = 0.5V, OUTB(1) VOL = 0.2V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN072:
  Functional:     No functional failures.
  ICC:            High ICC (7X) corresponds to OKC high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL (10-80X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal except for OKC N-channel test = 0.04V.
  Output Voltage: VOH = 4.3V for OKC, VOL = 0.2V for OKC,
                  VOL = 0.1V for OUTC(9:0), all nominal for TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN075:
  Functional:     Failed pin:  OUTB(2).
  ICC:            ICC high (10X) corresponding to OUTB(2) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, many IOL high (2-8X) on both vehicles.
  Prop Delays:
  Clamp Diodes:   Nominal except OUTB(2) N-channel test = 0.003V.
```

```
  Output Voltage: Nominal except OUTB(2) VOH = 0.6V, VOL = 0.2V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN076:
  Functional:     Failed pin:  OUTB(2).
  ICC:            ICC high (10X) corresponding to OUTB(2) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL high (100X) for OUTB(2).
  Prop Delays:
  Clamp Diodes:   Nominal except OUTB(2) N-channel test = 0.003V.
  Output Voltage: Nominal except OUTB(2) VOH = 0.6V, VOL = 0.3V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN077:
  Functional:     No functional failures.
  ICC:            ICC high (3X) corresponding to OKC high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL (10-30X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal except OKC N-channel test = 0.06V.
  Output Voltage: Nominal except OKC VOH = 4.7V, VOL = 0.15V.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN078:
  Functional:     No functional failures.
  ICC:            ICC high (3X) with definite pattern that does not
                  correspond to any input or output pin.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (2-3X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN090:
  Functional:     No functional failures.
  ICC:            ICC high (2-3X) corresponds to state of S1, S0.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (5X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN093:
  Functional:     No functional failures.
  ICC:            ICC high (2X) does not correspond to any pins.
```

Input Current: Nominal.
Output Current: IOH nominal, IOL nominal except (2X) for OUTB(1), OKB, OKC.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: Probable I/O damage.

SN099:
Functional: No functional failures.
ICC: ICC high (2X) corresponds to toggling CMP bus.
Input Current: Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (2X) for some TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: Probable I/O damage.

SN100:
Functional: No functional failures.
ICC: ICC high (2X) does not correspond to any pins.
Input Current: Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (2X) for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: Probable I/O damage.

SN126:
Functional: No functional failures.
ICC: ICC high (2X) does not correspond to any pins.
Input Current: Nominal.
Output Current: IOH nominal, IOL (3X) for TVC, nominal for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: Probable I/O damage.

SN137:
Functional: No functional failures.
ICC: ICC high (2X) does not correspond to any pins.
Input Current: IIH nominal. IIL nominal except (2X) on CMP(3).
Output Current: IOH nominal, IOL nominal except for (2X) on OUTB(1), OKB, OKC.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.

```
  PROGNOSIS:       Probable I/O damage.
-------------------------------------------------------------------------
SN201:
  Functional:      Failed pin:  OUTB(4).
  ICC:             ICC high (10X) corresponding to OUTB(4) high.
  Input Current:   Nominal.
  Output Current:  IOH nominal, IOL (100X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH = 0.5V for OUTB(4), VOL = 0.2 for many TVC pins.
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
SN205:
  Functional:      No functional failures.
  ICC:             ICC high (2X) throughout the pattern set.
  Input Current:   Nominal.
  Output Current:  IOH nominal. IOL (2-3X) for many pins.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  Nominal.
  PROGNOSIS:       Probable I/O damage.
-------------------------------------------------------------------------
SN206:
  Functional.      Failed pins:  All TVB pins.
  ICC:             ICC high (15X) partially corresponds with OUTB(0) low.
  Input Current:   IIH (3X) for INB(3), S0. IIL (1.5X) for CMP(0).
  Output Current:  IOH nominal. IOL nominal for TVC, (4X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH nominal except (0.5V) for OUTB(3,7).
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
SN207:
  Functional:      No functional failures.
  ICC:             ICC high (8X) partially corresponds with OUTB(0) low.
  Input Current:   IIH nominal. IIL nominal except (2X) for CMP(0).
  Output Current:  IOH nominal. IOL nominal except (2X) for OKB, OKC,
                   and OUTB(1).
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  Nominal.
  PROGNOSIS:       Probable I/O damage.
-------------------------------------------------------------------------
SN210:
  Functional.      No functional failures.
  ICC:             ICC high (2X) partially corresponds with OUTB(0) high.
  Input Current:   Nominal.
```

```
  Output Current: IOH nominal. IOL nominal for TVC, (2-4X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN212:
  Functional:     No functional failures.
  ICC:            ICC high (2X) does not correspond to any pins.
  Input Current:  Nominal.
  Output Current: IOH nominal. IOL (2-3X) for many pins.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN213:
  Functional:     No functional failures.
  ICC:            ICC somewhat high (1.5X) does not correspond to any
                  pin.
  Input Current:  Nominal.
  Output Current: IOH nominal. IOL nominal for TVC, (2X) for OUTB(1),
                  OKB, and OKC.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN214:
  Functional:     No functional failures.
  ICC:            ICC somewhat high (1.5X) does not correspond to any
                  pin.
  Input Current:  Nominal.
  Output Current: IOH nominal. IOL nominal for TVC, (2X) for OUTB(1),
                  OKB, and OKC.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      Probable I/O damage.
-------------------------------------------------------------------------
SN218:
  Functional:     Failed pins:  All TVB pins.
  ICC:            ICC high (15X) corresponding to (S1 high and S0 low).
  Input Current:  IIH (3X) for S1. All else nominal.
  Output Current: IOH nominal.  IOL nominal for TVC, (2-3X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
```

```
  Output Voltage: Nominal.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN219:
  Functional:     Failed pins:  All TVB pins.
  ICC:            ICC high (15X) corresponding to (S1 high and S0 low).
  Input Current:  IIH (3X) for S1.  All else nominal.
  Output Current: IOH nominal.  IOL nominal for TVC, (2-4X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN220:
  Functional:     No functional failures.
  ICC:            ICC high (2X) corresponding to S1 low (no stress).
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (6X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: Nominal.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN278:
  Functional:     Failed pin:  OUTB(4).
  ICC:            ICC high (10X) corresponding to OUTB(4) low.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal except for OUTB(4) (1000X)
  Prop Delays:
  Clamp Diodes:   Output N-channel test for OUTB(4) = 0.002V,
                  all other tests nominal.
  Output Voltage: VOH nominal, VOL nominal except for OUTB(4) = 4.4V
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN282:
  Functional:     Failed pin: OKC.
  ICC:            ICC high (10X) corresponding to OKC high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL (100X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:   Output N-channel test = 0.003V for OKC, all other
                  test nominal.
  Output Voltage: VOH nominal except (0.6V) for OKC,
                  VOL (0.1V) for TVC, nominal for TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN285:
```

Functional: Failed pins: All except OK.
ICC: ICC high (40X) corresponding to S1 high (stress).
Input Current: IIH (10X) for S0. All else nominal.
Output Current: Nominal.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: I/O damage.

SN289:
Functional: No funct'onal failures.
ICC: ICC high (2X) corresponding to S1 high (stress).
Input Current: Nominal.
Output Current: IOH nominal. IOL (2X) for OUTB(1), OKB, OKC.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: I/O damage. Probable stress control damage.

SN292:
Functional: Failed pins: All TVB pins.
ICC: ICC high (15X) corresponding to S1 low (no stress).
Input Current: IIH (2-4X) for most inputs. IIL Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (30X) for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: VOH nominal, VOL nominal for TVC, (0.07V) for TVB.
PROGNOSIS: I/O damage.

SN294:
Functional: No functional failures.
ICC: ICC high (2X) corresponding to S1 low (no stress).
Input Current: Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (4X) for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: I/O damage. Probable stress control damage.

SN297:
Functional: No functional failures.
ICC: ICC high (10X) corresponding to S1 low (no stress).
Input Current: IIH (3X) for S1. IIL (2X) for CMP(0).
Output Current: IOH nominal, IOL nominal for TVC, (20X) for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: VOH nominal, VOL nominal for TVC, (0.06V) for TVB.

PROGNOSIS: I/O damage. Probable stress control damage.

SN298:

Functional: Failed pins: OUTB(0,4,5,7,8), OKB, OK.
ICC: ICC high (10X) corresponding to S1 low (no stress).
Input Current: Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (30X) for TVB.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: VOH nominal, VOL nominal for TVC, (0.07V) for TVB.
PROGNOSIS: I/O damage. Probable stress control damage.

SN300:

Functional: Failed pins: All TVB pins, OKC.
ICC: ICC high (40X) throughout the pattern set.
Input Current: IIH nominal, IIL nominal for TVC, (100X) for TVB.
Output Current: IOH nominal, IOL nominal for TVC, (1000X) for TVB.
Prop Delays:
Clamp Diodes: Input N-channel test = 1.2V for TVB. All else nominal.
Output Voltage: VOH (4.7V) for all, VOL nominal for TVC,
(1.3V) for TVB.
PROGNOSIS: I/O damage.

SN301:

Functional: Failed pins: All TVB pins.
ICC: ICC high (30X) corresponding to S1 high (stress).
Input Current: Nominal.
Output Current: IOH nominal, IOL nominal for TVC, (20X) for TVB.
Prop Delays:
Clamp Diodes: Input N-channel test = 1.2V for TVB. All else nominal.
Output Voltage: VOH nominal, VOL nominal for TVC, (1.5V) for TVB.
PROGNOSIS: I/O damage. Probable stress control damage.

SN302:

Functional: Failed pins: All except OK.
ICC: ICC high (40X) corresponding to S1 high (stress).
Input Current: IIH (10X) for S0. All else nominal.
Output Current: Nominal.
Prop Delays:
Clamp Diodes: Nominal.
Output Voltage: Nominal.
PROGNOSIS: I/O damage.

SN304:

Functional: Failed pins: All TVB pins.
ICC: ICC high (20X) throughout the pattern set.
Input Current: Nominal.

```
  Output Current: IOH nominal, IOL nominal for TVC, (40X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, (0.8V) for TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN305:
  Functional:     No functional failures.
  ICC:            ICC high (40X) corresponding to S1 high (stress).
  Input Current:  IIH (4X) for CK, S1, (10X) for S0.
                  IIL (2X) for CMP(0).
  Output Current: IOH nominal, IOL nominal for TVC, (30X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, (0.7V) for TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN306:
  Functional:     Failed pins:  All except OUTC(2,6,9).
  ICC:            ICC high (40X) throughout the pattern set.
  Input Current:  IIH (400X) for TVC, (100X) for TVB.
                  IIL nominal for TVC, (100X) for TVB.
  Output Current: IOH nominal, IOL nominal for TVC, (1000X) for TVB.
  Prop Delays:
  Clamp Diodes:   Input N-channel test = 1.2V for TVB. All else nominal.
  Output Voltage: VOH low (4.7) for all, VOL nominal for TVC,
                  high (3.0V) for TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN307:
  Functional:     Failed pins:  All TVB pins, OKC.
  ICC:            ICC high (10X) throughout pattern set. (20X)
                  corresponding to OKC or OKB high. (40X) with no
                  correlation to any pin.
  Input Current:  IIH nominal, IIL nominal for TVC, (40X) for TVB.
  Output Current: IOH nominal, IOL (100X) for TVC, (500X) for TVB.
  Prop Delays:
  Clamp Diodes:   Input N-channel test nominal for TVC, (0.4V) for TVB.
                  All other tests nominal.
  Output Voltage: VOH low (4.7V) for all, OKC VOH = 0.6V.
                  VOL (0.1V) for TVC, (2.5V) for TVB.
  PROGNOSIS:      I/O damage.  See failure analysis report SPL11659.
-------------------------------------------------------------------------
SN308:
  Functional:     No functional failures.
  ICC:            ICC high (4X) corresponding to S1 low (no stress).
  Input Current:  IIH (2X) for all. IIL nominal.
```

```
  Output Current: IOH nominal, IOL nominal for TVC, (10X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, (0.4V) for TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN309:
  Functional:     No functional failures.
  ICC:            ICC high (5X) corresponding to S1 low (no stress).
  Input Current:  IIH (2X) for all. IIL nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (15X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, (0.4V) for TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN310:
  Functional:     Failed pin:  OUTB(9).
  ICC:            ICC high (10X) corresponding to OUTB(9) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (20X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal except for OUTB(9) VOH = 0.4V.
                  VOL nominal for TVC, (0.6V) for TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN313:
  Functional:     No functional failures.
  ICC:            ICC high (8X) corresponding to S1 low (no stress).
  Input Current:  IIH (2X) for all. IIL nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (20X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL high (0.6V) for TVB.
  PROGNOSIS:      I/O damage. Probable stress control damage.
-------------------------------------------------------------------------
SN315:
  Functional:     Failed pins: OUTB(0,4,5,7), OK, OKB.
  ICC:            ICC high (10X) throughout. (20X) corresponding to
                  S1 low (no stress).
  Input Current:  IIH (2X) for all, (4X) for S1. IIL nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (20X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL high (0.07V) for TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
```

SN317:

Functional:	Failed pins: All TVB pins, OKC.
ICC:	ICC high (40X) throughout pattern set.
Input Current:	IIH nominal, IIL nominal for TVC, (60X) for TVB.
Output Current:	IOH nominal, IOL nominal for TVC, (1000X) for TVB.
Prop Delays:	
Clamp Diodes:	Input N-channel test nominal for TVC, (1.2V) for TVB. All other tests nominal.
Output Voltage:	All VOH low (4.7V), VOL = 2.3V for TVB.
PROGNOSIS:	I/O damage.

SN318:

Functional:	Failed pins: All TVB pins, OKC.
ICC:	ICC high (40X) throughout pat ern set.
Input Current:	IIH nominal, IIL nominal for TVC, (100X) for TVB.
Output Current:	IOH nominal, IOL nominal for TVC, (1000X) for TVB.
Prop Delays:	
Clamp Diodes:	Input N-channel test nominal for TVC, (1.2V) for TVB. All other tests nominal.
Output Voltage:	All VOH low (4.7V), VOL = 2.3V for TVB.
PROGNOSIS:	I/O damage.

SN319:

Functional:	No functional failures.
ICC:	ICC high (40X) corresponding to S1 high (stress).
Input Current:	IIH (2X) for all, (10X) for S0.IIL nominal.
Output Current:	IOH nominal, IOL nominal for TVC, (30X) for TVB.
Prop Delays:	
Clamp Diodes:	Nominal.
Output Voltage:	VOH nominal, VOL nominal for TVC, (0.7V) for TVB.
PROGNOSIS:	I/O damage. Probable stress control damage.

SN320:

Functional:	Failed pins: All except OUTC(9:7).
ICC:	ICC high (20X) corresponding to OKC or OKB high. ICC high (40X) corresponding to S1 high (stress).
Input Current:	IIH nominal, IIL nominal for TVC, (10X) for TVB.
Output Current:	IOH nominal, IOL nominal for TVC, (100X) for TVB.
Prop Delays:	
Clamp Diodes:	S1 N-channel test = 0.9V, all else is nominal.
Output Voltage:	TVC nominal, TVB VOL = 1.0V, OUTB(9) VOH = 2.3V
PROGNOSIS:	I/O damage. Probable stress control damage.

SN321:

Functional:	Failed pins: All of TVB.
ICC:	ICC high (15X) corresponds to S1 low (no stress).

```
  Input Current:  IIH (3X) for all except S0. IIL nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (30X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL nominal for TVC, VOH = 0.7V for TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN322:
  Functional:     Failed pins:  OUTB(9).
  ICC:            ICC high (20X) corresponds to OUTB(9) high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (10X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH = 0.4V for OUTB(9), VOL = 0.6V for much of TVB.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN323:
  Functional:     Failed pins:  All of TVB.
  ICC:            ICC high (15X) corresponds to S1 low (no stress).
  Input Current:  IIH (3X) for all except S0. IIL nominal.
  Output Current: IOH nominal, IOL nominal for TVC, (40X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH nominal, VOL = 0.7V for much of TVB.
  PROGNOSIS:      I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN324:
  Functional:     No functional failures.
  ICC:            ICC high (4X) corresponds partially with OKC high.
  Input Current:  Nominal.
  Output Current: IOH nominal, IOL (30X) for TVC, nominal for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal.
  Output Voltage: VOH = 4.7V for OKC, VOL = 0.6V for many from TVC.
  PROGNOSIS:      I/O damage.
-------------------------------------------------------------------------
SN325:
  Functional:     Failed pins:  OKC.
  ICC:            ICC high (20X) corresponding to OKC high,
                  ICC high (40X) corresponding to S1 high (stress).
  Input Current:  IIH (3X) for all, (10X) for S0. IIL nominal.
  Output Current: IOH nominal, IOL (100X) for TVC, (40X) for TVB.
  Prop Delays:
  Clamp Diodes:   Nominal except for OKC N-channel test = 0.03V.
  Output Voltage: VOH nominal except OKC = 0.6V, VOL = 0.1V for many
                  from both TVC and TVB.
```

```
  PROGNOSIS:       I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN326:
  Functional:      No functional failures.
  ICC:             ICC high (4X) corresponding to S1 low (no stress).
  Input Current:   IIH (2X) for all except S0. IIL nominal.
  Output Current:  IOH nominal, IOL nominal for TVC, (10X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH nominal, VOL nominal for TVC, VOL = 0.04V for TVB.
  PROGNOSIS:       I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN327:
  Functional:      No functional failures.
  ICC:             ICC high (4X) corresponding to S1 low (no stress).
  Input Current:   IIH (2X) for all except S0. IIL nominal.
  Output Current:  IOH nominal, IOL nominal for TVC, (10X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH nominal, VOL nominal for TVC, VOL = 0.04V for TVB.
  PROGNOSIS:       I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN328:
  Functional:      Failed pins:  All TVB outputs, OKC, and OUTC(1).
  ICC:             ICC high (50X) throughout pattern set.
  Input Current:   IIH nominal, IIL nominal for TVC, (30X) for TVB.
  Output Current:  IOH nominal, IOL (100X) for TVC, (1000X) for TVB.
  Prop Delays:
  Clamp Diodes:    Input N-channel test = 1.0V for S1, S0, and INB(4:0).
                   Output N-channel test = 0.003V for OUTC(1).
                   Output P-channel test nominal.
  Output Voltage:  VOH =4.7V for all except OUTC(1) = 0.6V OK,CKB = 1.8V.
                   VOL = 0.2V for much of TVC, VOL = 2.5V for TVB.
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
SN329:
  Functional:      Failed pins:  All TVB outputs and OKC.
  ICC:             ICC high (30-40X) throughout pattern set.
  Input Current:   IIH nominal, IIL nominal for TVC, (50X) for TVB.
  Output Current:  IOH nominal, IOL nominal for TVC, (1000X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal except for TVB input N-channel test = 1.3V.
  Output Voltage:  All VOH about 4.7V, VOL for TVB = 2.5V.
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
SN330:
  Functional:      Failed pins:  All TVB outputs.
```

```
  ICC:             ICC high (10X) corresponding to S1 low (no stress).
  Input Current:   IIH (3X) for all except S0.IIL nominal.
  Output Current:  IOH nominal, IOL nominal for TVC, (4X) for all TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  VOH somewhat low for all, VOL nominal for TVC,
                   VOL = 0.1V for TVB.
  PROGNOSIS:       I/O damage.  Probable stress control damage.
-------------------------------------------------------------------------
SN331:
  Functional:      No functional failures.
  ICC:             ICC high (2X) does not correspond with any pin.
  Input Current:   Nominal.
  Output Current:  IOH nominal, IOL nominal for TVC, (3X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  Nominal.
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
SN348:
  Functional:      Failed pin:  OKB.
  ICC:             ICC high (10X) corresponding to OKB high.
  Input Current:   Nominal.
  Output Current:  IOH nominal, IOL nominal for TVC, (10-100X) for TVB.
  Prop Delays:
  Clamp Diodes:    Nominal except OKB N-channel test = 0.003V.
  Output Voltage:  VOH = 0.5V for OKB, VOL = 0.1V for several TVB pins.
  PROGNOSIS:       I/O damage.
-------------------------------------------------------------------------
```

#
LIST OF FAILURE MODES NOTED FOR FAILED
RLOSTV DEVICES BASED ON ELECTRICAL
CHARACTERIZATION.
#

---

1. High IOL for TVB or TVC.

SN001, SN002, SN006, SN011, SN020, SN078, SN099, SN100, SN126, SN205, SN210, SN212, SN213, SN214, SN297, SN298, SN300, SN301, SN304, SN331.

---

2. High ICC correlated to stress mode.

SN010, SN090, SN220, SN289, SN294.

---

3. High ICC correlated to damaged I/O.

SN059, SN066, SN071, SN072, SN075, SN076, SN077, SN206, SN207, SN218, SN219, SN278, SN282, SN285, SN292, SN305, SN306, SN307, SN308, SN309, SN310, SN313, SN315, SN317, SN318, SN319, SN320, SN321, SN322, SN323, SN324, SN325, SN326, SN327, SN328, SN329, SN330, SN348.

---

4. High ICC correlated to undamaged I/O.

SN056*, SN201*, SN302*.

---

4. High ICC not correlated to any I/O.

SN093*, SN137*.

---

* Selected for destructive physical analysis.

In order to better understand the probable cause of damage to the input/output cells during the screen and lifetest, we have counted the number of failures noted for each pin in the design. This helps to determine if the majority of pin failures occurred during handling or while the parts were in the screen/lifetest boards. If the failures were due to handling, i.e. electrostatic discharge (ESD) damage, the pin failures should be distributed fairly randomly throughout the part. At worst, a couple of pins located at the top and bottom of the package which frequently come in to contact with the fingers of the operater during handling should display a high number of failures. This is not at all what is observed here.

On almost all of the failed parts, the outputs of Test Vehicle B (OKB, and OUTB) are damaged. Moreover, it is not any one pin but instead the entire bank of outputs which are damaged most of the time. In fact, the outputs of Test Vehicle B are damaged roughly four times as frequently as the outputs of Test Vehicle C.

The input pins were not damaged as frequently as the outputs, but again the inputs of Test Vehicle B were damaged approximately four times as frequently as the inputs of Test Vehicle C.

This systematic (as opposed to random) failures of the input pins definitely point to damage incurred while the devices were situated in the test boards. It is suspected that while some damage occurred due to voltage spikes from an unconditioned power outlet early in the lifetest, the majority of failures are due to inherent weakness in Test Vehicle B (caused by the unique stress control circuitry) which became apparent during the extended voltage overstress presented by the lifetest. While some pins may have been damaged by ESD, this appears not to be a major cause of failures during the lifetest.

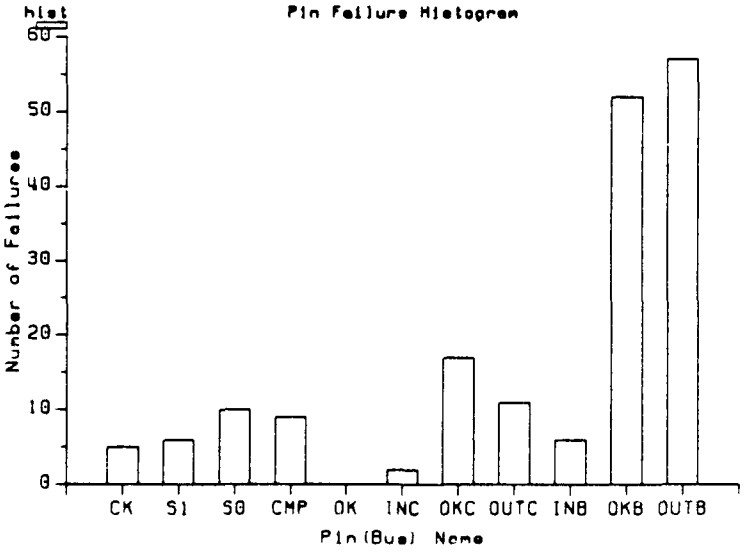


Figure 70 Number of Damaged I/O for Each Pin

9.2 Destructive Physical Analysis Results

Of the 68 parts which participated in the electrical data analysis portion of the failure analysis, only serial numbers 056, 201, 302, 093, and 137 were selected to undergo limited destructive physical analysis (DPA) since they displayed electrical characteristics which could not be categorized as I/O pin failures. Unfortunately, programmatic constraints limited this DPA to a brief electrical and visual inspection. The results of these DPA's are outlined on the following pages. TDDB was eliminated as the cause of failure in all parts except serial numbers 093 and 137.

9.2.1 Serial Number 056

9.2.1.1 Electrical Characterization Summary

```
SN056:
  Functional:      Failed pin: OUTB(7).
  ICC:             High ICC (20X) corresponding to OKB high.
  Input Current:   IIH (3X) for INB(3) and S0. IIL (4X) for CMP(0).
  Output Current:  IOH nominal, IOL high (20X) for many pins.
  Prop Delays:
  Clamp Diodes:    Nominal.
  Output Voltage:  Many out of spec.  OUTB(7) VOH = 0.5V.
```

9.2.1.2 Destructive Physical Analysis

1. Input pin 39, CMP(0) was shorted to VDD1. This short is shown in figure 71.

2. Output pin 31, OUTB(0) was shorted to VSS2. Figure 72 shows the source of the output n-channel transistor shorted to the drain.

3. Output pin 40, OKC was shorted to VSS1. Figure 73 shows a surface track shorting the source of the output n-channel transistor to the drain.

4. Output pin 21, OUTB(7) was shorted to VSS2. Figure 74 shows a surface track shorting the source of the output n-channel transistor to the drain.

9.2.1.3 Conclusion

The source to drain shorts were caused by a high-voltage/low-energy overstress event inconsistent with TDDB. Either electrical overstress or ESD damage is possible.

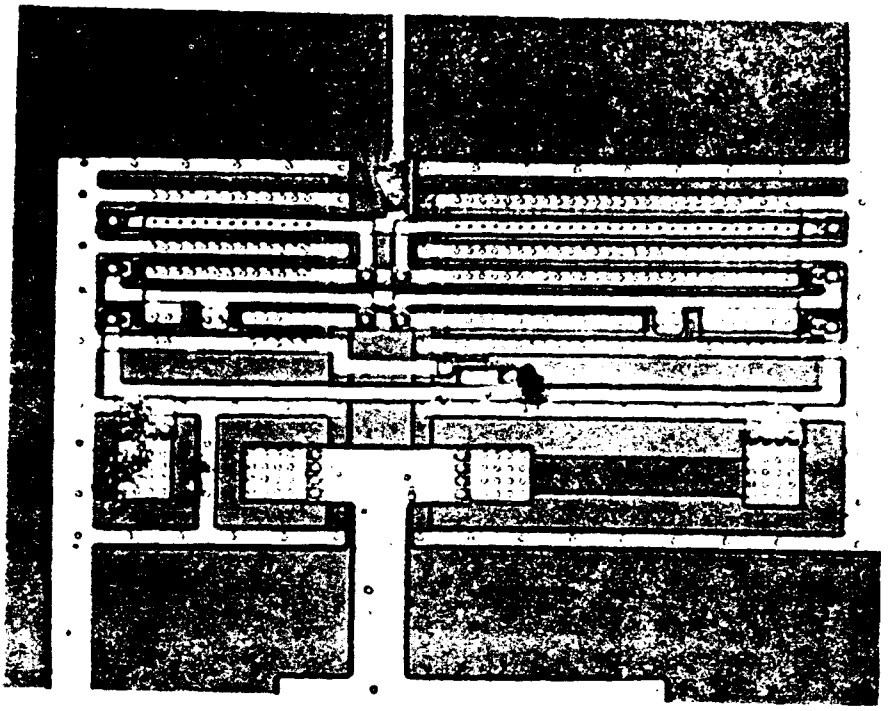


Figure 71 SN056, Pin 39: Input Pad Short

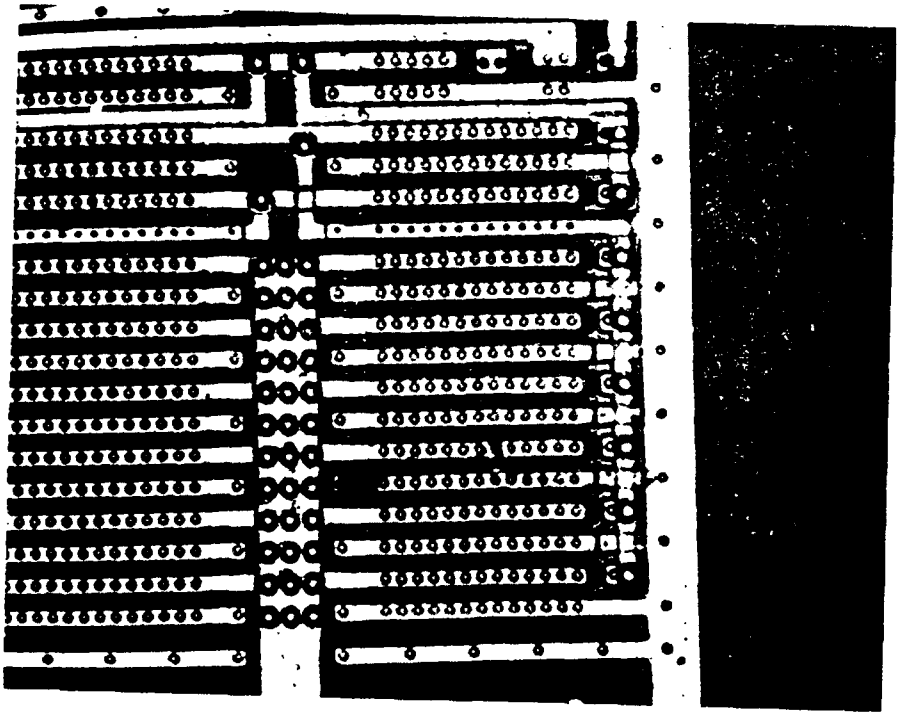


Figure 72 SN056, Pin 31: Output Pad Short

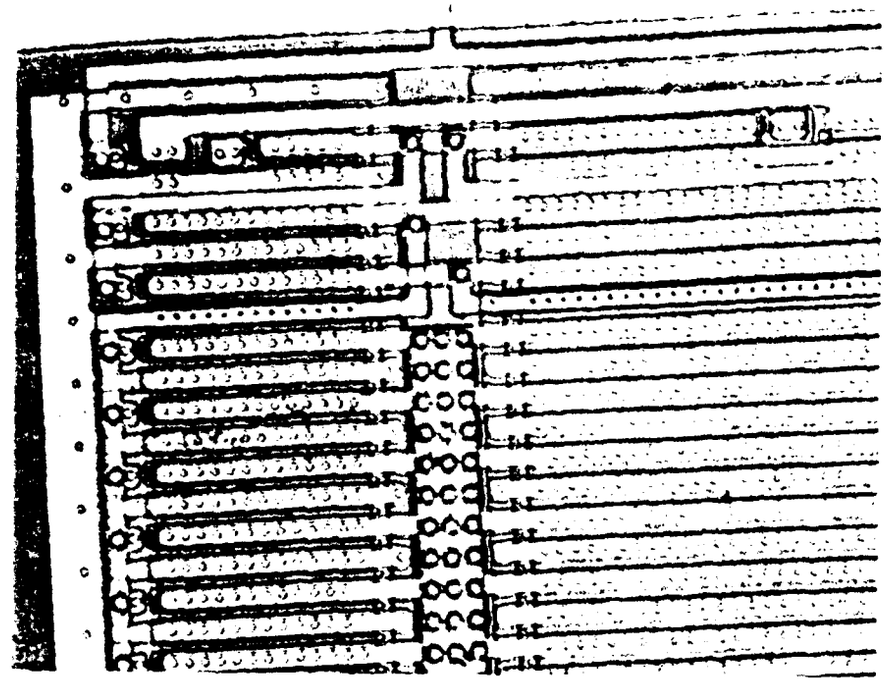


Figure 73 SN056, Pin 40: Output Pad Short

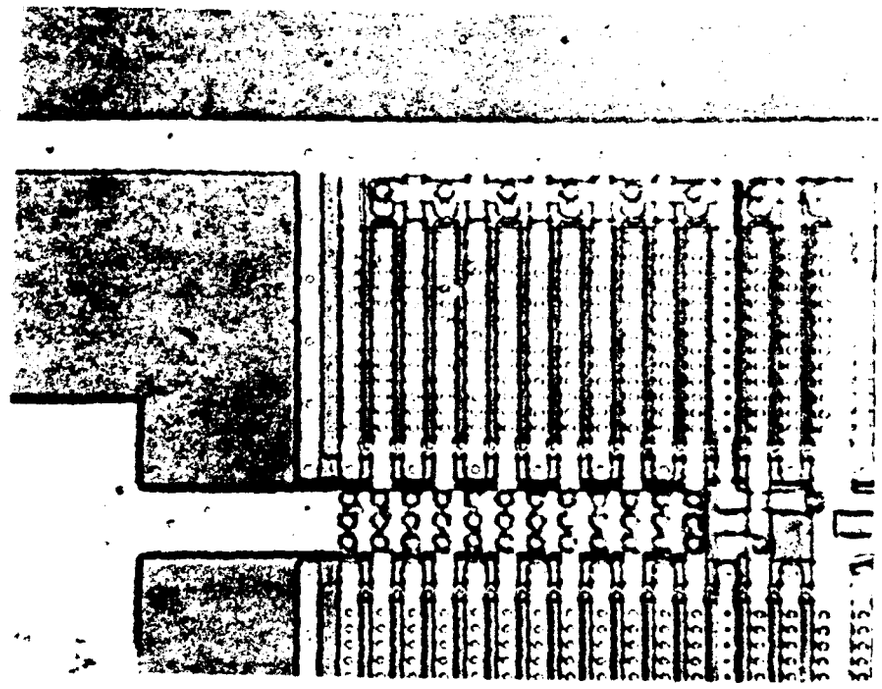


Figure 74 SN056, Pin 21: Output Pad Short

9.2.2 Serial Number 093

9.2.2.1 Electrical Characterization Summary

SN093:

Functional:	No functional failures.
ICC:	ICC high (2X) does not correspond to any pins.
Input Current:	Nominal.
Output Current:	IOH nominal, IOL nominal except (2X) for OUTB(1), OKB, OKC.
Prop Delays:	
Clamp Diodes:	Nominal.
Output Voltage:	Nominal.

9.2.2.2 Destructive Physical Analysis

No visual anomalies with pin OUTB(1). No electrical anomalies with pin OUTB(0) but visual inspection reveals anomalies which are perhaps consistent with gate oxide damage.

9.2.2.3 Conclusion

The anomalies with pin OUTB(0) are minor. If there were gate oxide damage as alluded to in the DPA, this would clearly show up in the electrical characterization. However, no electrical anomalies are found with this pin. No conclusions are available as a result of this analysis.

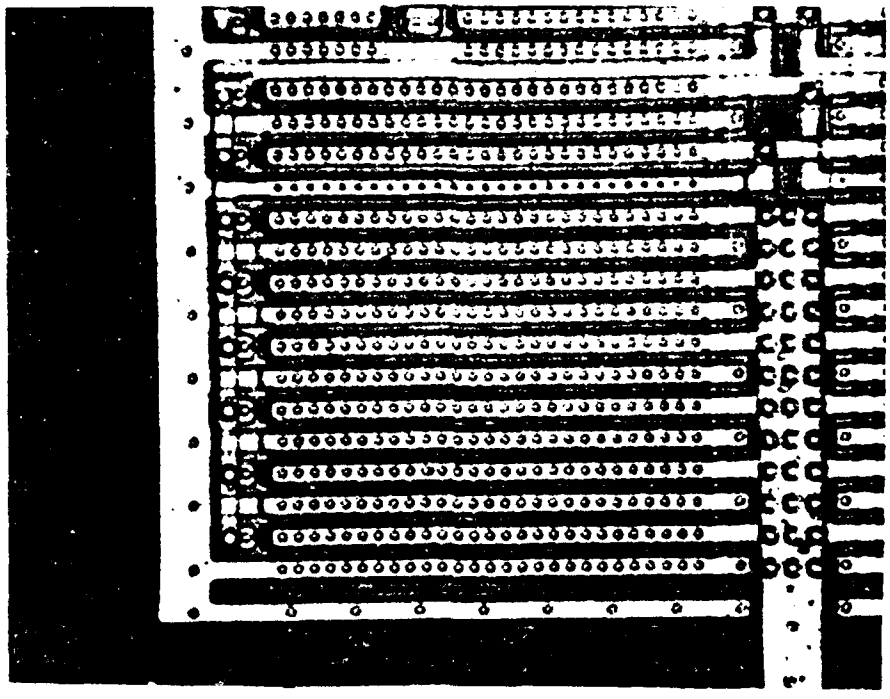


Figure 75 SN093, Pin 31: Output Pad Visual Anomalies

9.2.3 Serial Number 137

9.2.3.1 Electrical Characterization Summary

SN137:

Functional:	No functional failures.
ICC:	ICC high (2X) does not correspond to any pins.
Input Current:	IIH nominal. IIL nominal except (2X) on CMP(3).
Output Current:	IOH nominal, IOL nominal except for (2X) on OUTB(1), OKB, OKC.
Prop Delays:	
Clamp Diodes:	Nominal.
Output Voltage:	Nominal.

9.2.3.2 Destructive Physical Analysis

No visual anomalies found.

9.2.3.3 Conclusion

No conclusions available as a result of failure analysis.

9.2.4 Serial Number 201

9.2.4.1 Electrical Characterization Summary

SN201:

Functional:	Failed pin: OUTB(4).
ICC:	ICC high (10X) corresponding to OUTB(4) high.
Input Current:	Nominal.
Output Current:	IOH nominal, IOL (100X) for TVC, nominal for TVB.
Prop Delays:	
Clamp Diodes:	Nominal.
Output Voltage:	VOH = 0.5V for OUTB(4), VOL = 0.2 for many TVC pins.

9.2.4.2 Destructive Physical Analysis

1. Pin 25, OUTB(4) shorted to VSS2. Visual inspection revealed a surface track shorting the source of the n-channel output transistor to the drain.

9.2.4.3 Conclusion

This part was incorrectly categorized during the electrical data analysis. It should have been categorized as 'High ICC correlated to a damaged I/O. The n-channel transistor source/drain short was caused by a high-voltage/low-energy overstress event. This damage is not consistent with TDDB.

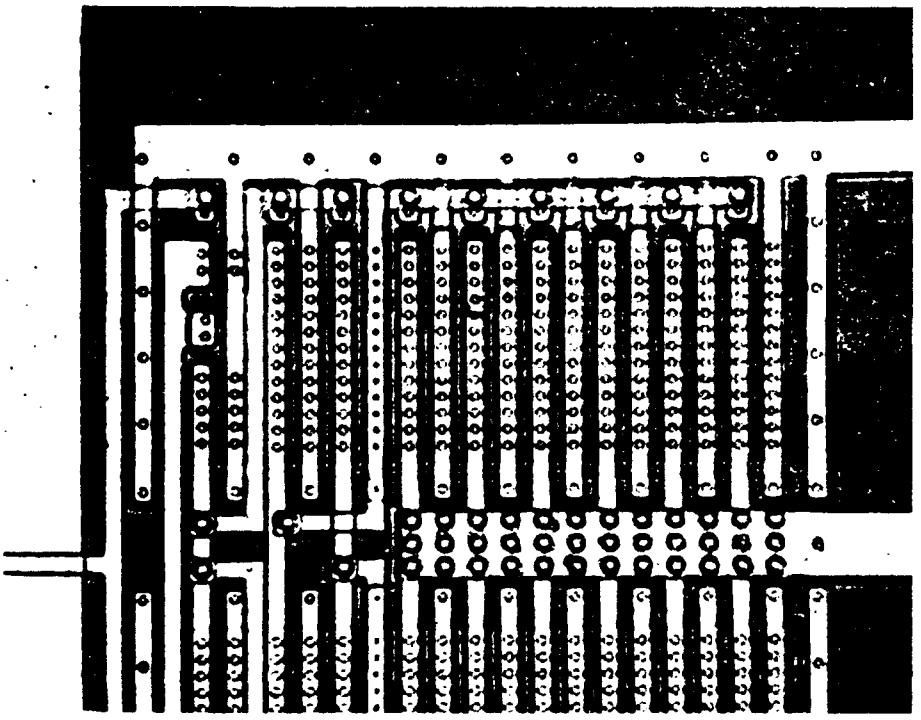


Figure 76 SN201, Pin 25: Output Pad Short

9.2.5 Serial Number 302

9.2.5.1 Electrical Characterization Summary

SN302:

Functional:	Failed pins: All except OK.
ICC:	ICC high (40X) corresponding to S1 high (stress).
Input Current:	IIH (10X) for S0. All else nominal.
Output Current:	Nominal.
Prop Delays:	
Clamp Diodes:	Nominal.
Output Voltage:	Nominal.

9.2.5.2 Destructive Physical Analysis

1. Visual examination revealed burn on drain finger of n-channel transistor driving stress control signal SB.

9.2.5.3 Conclusion

This part was incorrectly categorized during the electrical data analysis. In fact the high ICC is directly correlated to stress mode. The n-channel burn is caused by high sustained current due to a drain/pwell junction breakdown. ESD damage is eliminated because this transistor connects only to internal devices on the chip. Also, TDDB is unlikely since this failure mode occurs on 5 other failed devices.

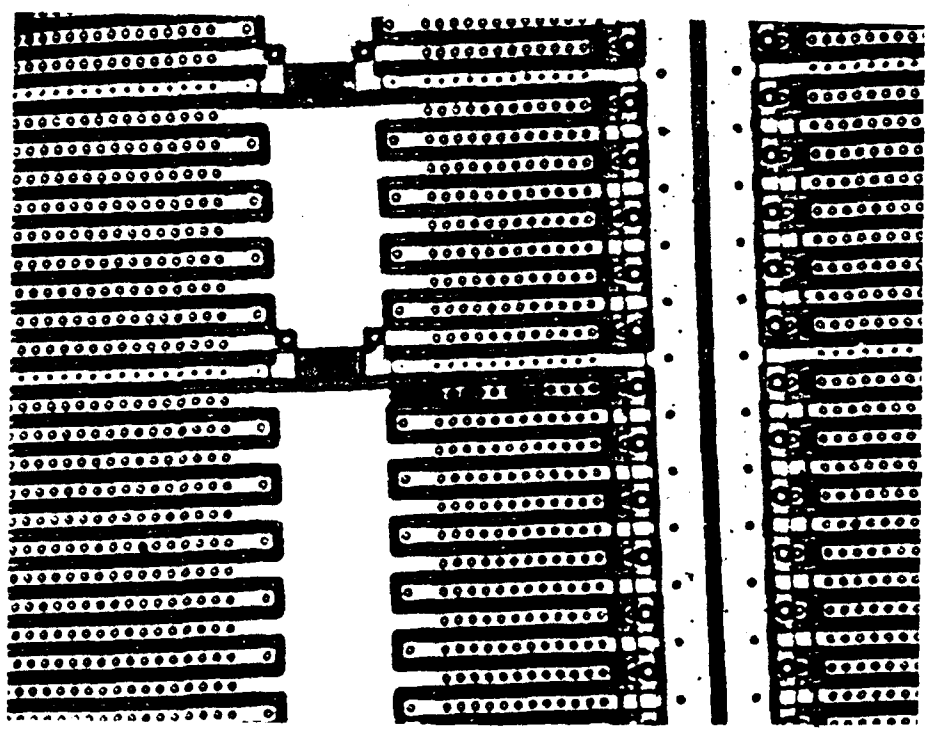


Figure 77 SN302: Stress Control (SB) Damage

10. Conclusions

The objective of this study was to determine and evaluate new methods of applying reliability screen tests to CMOS random logic integrated circuits in order to reduce the incidence of in-field failures due to time dependent dielectric breakdown. The study was broken down into three major subtasks: oxide modeling, screening technique development, and test.

10.1 Oxide Modeling

Special test structures (capacitors) were fabricated and tested to measure the characteristics of a particular gate oxide. The testing performed was ramp voltage breakdown measurements and data analysis. These tests provided data that is consistent with other published results and indicates that the gate oxide is of good quality and that the cumulative percent failures follows a logarithmic relationship with area. This portion of the study provided useful information on the characteristics of the gate oxide process. Some example results of this modeling effort, showing the instantaneous failure rate of a particular size test capacitor as a function of applied electric field are displayed in figure 78.

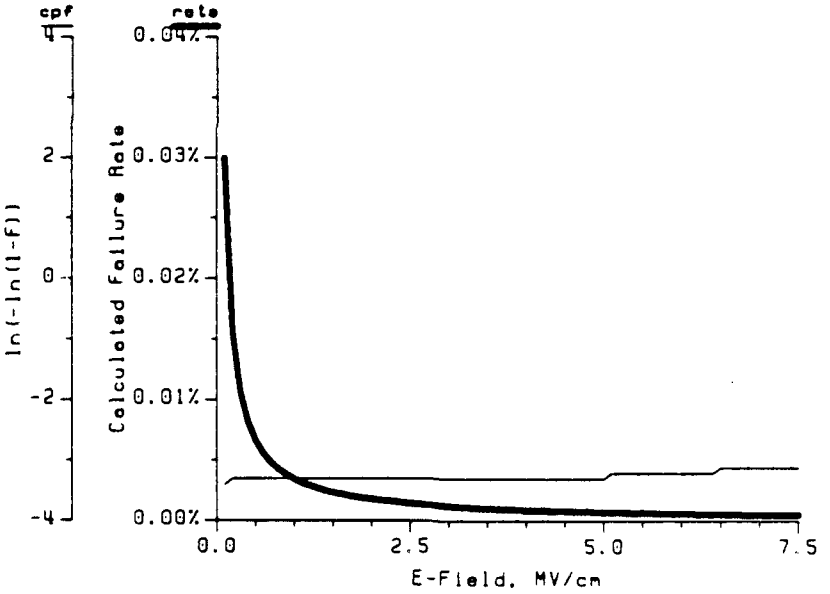


Figure 78 Failure Rate Curve for Test Capacitor "C"

10.2 Screening Techniques

This task involved the development of methods to improve oxide reliability screen tests for random logic circuitry. Two methods were studied: a vector set optimization task and the addition of internal circuitry.

The first method involved the optimization of the vector set to produce an equivalent amount of field stress on all of the gate oxide areas on the circuit. This task required unique software to assess the stress produced by the vector set. This was developed and is referred to as the Oxide Stress Analyzer program. The data produced was shown on a Stress Histogram. These two elements are very useful for assessing and understanding the uniformity of the stress induced on a random logic circuit. They worked well and provided insight into the extreme difficulty in producing identical stress levels for all oxide areas.

Even though it is not possible to stress all areas identically it may be possible to develop a test pattern set that at least stresses each gate oxide area once. This would be greatly aided by the use of testability scan paths to break a device up into smaller blocks of random logic. A test at an elevated voltage level improves the reliability of devices that are subjected to it and pass.

The second method involved the addition of circuitry on the device that would only be functional during the oxide screening portion of the device manufacturing. A custom circuit was designed and built that allowed each of the gates on the device to be taken high or low independently. The function of the circuitry to provide equivalent screening levels worked properly and is a valid concept. However, we feel that this approach is too costly in terms of both device performance and die area. A 100% performance penalty coupled with a 75% die area penalty was incurred. This is an unacceptable cost for the expected slight increase in reliability.

10.3 Test

The test performed required the design and fabrication of an oxide reliability test vehicle. A portion of the test vehicles were subjected to the two screening methods developed and then these test vehicles and unscreened test vehicles were subjected to a 4000 hour accelerated life test. The acceleration factor utilized was an operating voltage of 8 volts.

The data developed during the oxide modeling was to be utilized to aid in the selection of the voltage stress to be used on the test vehicles. Unfortunately the foundry that supplied the capacitors for the oxide modeling closed and the test vehicles had to be obtained from a different foundry. The selection of the stress condition was then performed according to other circuit constraints. The avalanche breakdown voltage of the N+ drain to the P-well on the test vehicles was the limiting factor. This was approximately 9.5 volts. An 8 volt level was selected for the screen test (two hours of stress time on each device.) This provides a significant acceleration over the expected 5 volt operation. Assuming a conservative acceleration of 10^4/MV/cm, operation at 8 volts (8 volts / 225 Angstrom = 3.6 MV/cm) versus operation at 5 volts (5 volts / 225 Angstrom = 2.2 MV/cm) provides an acceleration factor of 13,600 times. For example the two hour screen at 8 volts is equivalent to over 3 years of operation at 5 volts. However, with the extremely low failure rate experienced due to TDDB this 8 volt screen did not produce any TDDB failures.

The 4000 hour life test was also run at an 8 volt level in an effort to keep the stress high enough to produce TDDB failures. Due to system transients and board problems there were a high number of failures during the testing unrelated to TDDB. There were a total of 260 parts

in the 4000 hour life test and estimates of the failure rates indicated that for TDDB there would be 0 to 2 parts fail. It is impossible to get statistically significant data with this number of failures. The test portion of this task provided little data other than information related to problems and solutions for prescreening and life testing this type of part.

10.4 Final Comments

This study provided useful TDDB ramp test data on test capacitors. Computer programs were developed that provide gate oxide stress information and a means to display it. A design scheme was developed and fabricated to allow more even stressing of random logic integrated circuit gate oxides. A screen and accelerated life test were performed that provided inconclusive results.

In all, this study has provided information to increase the knowledge and database in the area of TDDB for random logic integrated circuits.

A. Oxide Stress Analyzer Help File

```
                    Oxide Stress Analyzer
                    ---------------------

Author:    James M. Roucis

Date:      11-9-87

Location:  Martin Marietta, Denver Aerospace

  The following is a brief summary of the commands available in the Oxide
  Stress Analyzer (OSA).  Only the capitalized letters of a command need
  to be typed to initiate it.  Command line arguments that are surrounded
  by '<' and '>' indicate optional arguments.  A command line argument
  followed by '...' indicates that more than one argument may be given.
  All other arguments MUST be given on the command line.

  Comments on command lines start with '#' and end at the end of line.


Command         Action
-------         ------


CD  <Pathname>

              Set the current working directory.  This is similar to the
              Aegis "Working Directory" Command.  See the System Help
              directory for details (type HELP WD to an Aegis shell).



COllect  <-Time Range>  <-Charge Range>  <-Field Range>  Destination  Source

              This command interfaces the Oxide Stress Analyzer to the Oxide
              Stress Analyzer Stress Base (OSADB).  Stress is collected from the
              Stress base items specified by the pathname(s) in 'Source' and
```

placed into the Stress field of the plot object specified by the pathname 'Destination'. A thorough knowledge of Aegis pathname specification and wildcarding is essential for this command. The '-Time', '-Charge', and '-Field' options allow Stress to be collected from the Stress base that lies in a range of values specified by 'Range'. The format for the 'Range' specification is either a single value, or a minimum values followed immediatley by a ':' and a maximum value. Examples:

```
COLLECT  -TIME  10.5  TEN.FIVE_Stress  CMOSIIIC/SUBS/A.?*/?*

COLLECT  -CHARGE  2:12  CHARGE_Stress  CMOSIIIC/SUBS/A.?*/?*
```

COpy Source Destination

This command copies the plot object specified by 'Source' to a new plot object specified by 'Destination'. 'Source' must exist and 'Destination' must not be the name of a pre-existing plot object. This is the same command as 'CP'.

CP Source Destination

This command copies the plot object specified by 'Source' to a new plot object specified by 'Destination'. 'Source' must exist and 'Destination' must not be the name of a pre-existing plot object. This is the same command as 'COpy'.

CReate Pathname ...

This command creates the new plot object(s) specified by pathname(s) on the command line. The pathname(s) should not specify pre-existing plot objects.

DElete Pathname ...

This command deletes the plot object(s) specified on the command line. The plot object(s) specified should exist before deletion. Same action as the 'RM' command.

DO Pathname

Execute a list of commands from a file. 'Pathname' must be specified, and should be the name of file containing Oxide Stress Analyzer commands.

EXit

Exits the Oxide Stress Analyzer. Same action as the 'Quit' command.

HElp <Keyword>

Opens this read pad. If 'Keyword' is specified, 'Keyword' is searched for in the pad.

HIstory

Types to the screen a numbered listing of all commands entered to the Oxide Stress Analyzer. See below for the description of '!' (repeat a command).

LD <Options>

This is actually the Aegis LD ("List Directory") command. See the System Help directory for details on the <Options>

(type HELP LD to a shell). Same action as the 'LS' command.

LEast N Pathname Results

Sorts in increasing order the stress information found in the file 'Pathname' and writes a report of the first N gate areas in the file 'Results'.

LOck Pathname ...

Places a lock on the plot object(s) specified on the command line. The object(s) may not be plotted, removed, or deleted (see the 'PLot', 'DElete', and 'RM' commands). Use this as a safeguard for plot objects that you do not wish to change. See 'Unlock' for a description of removing the lock on a plot object or group of objects.

LR Pathname Plot-type Range Format <Result>

Performs linear-regression analysis on the plot information specified by 'Plot-type' in the object specified by 'Pathname'. The 'Plot-type' should be one of 'Mergedd', 'Cpfailure', or 'Ddensity'. 'Range' should specify the range of X values that the analysis will be performed on (see the description of the range format in 'COllect' above). 'Format' should be either 'Scalar' or 'Log'. 'Result' should be the name of a file where the analysis information will be printed. If this is not specified, the information will be printed to the screen.

LS <Options>

This is actually the Aegis LD ("List Directory") command. See the System Help directory for details on the <Options> (type HELP LD to a shell). Same action as the 'LD' command.

MErge Destination Pathname1 Pathname2 <...>

Merges defect density plots from 2 or more plot objects into the plot object specified by 'Destination'. This creates a file in the destination object called 'mergedd'. All of the objects to be merged, specified by 'Pathname1', 'Pathname2', etc., should contain a defect density plot.

MOst N Pathname Results

Sorts in decreasing order the stress information found in the file 'Pathname' and writes a report of the first N gate areas in the file 'Results'.

MV Source Destination

Changes the name of the plot object specified by the pathname 'Source' to the plot object specified by the pathname 'Destination'. Same action as the 'REname' command.

PLot Type Index Granularity Pathname

This command creates plot Stress for the object specified by 'Pathname'. The plot object must exist, and must contain collected Stress. See the description of the 'CReate' and 'COllect' commands. The 'Type' specifies what kind of analysis is to be performed on the object's Stress. This can be one of the following: 'Pfailure', 'Rcpfailure', 'Cpfailure', or 'Ddensity', corresponding to percent failure, raw cumulative percent failure, cumulative percent failure, and defect density, respectively. This parameter corresponds to the y-axis of the plot. The 'Index' specifies the part of the collected Stress to be analyzed. This can be one of the following: 'Time', 'Charge', or 'Field'. This parameter

corresponds to the x-axis of the plot. The 'Granularity' specifies the width of segments that the range of x values are divided into.

PWd

Prints the current working directory to the screen.

Quit

Quits the Oxide Stress Analyzer. Same action as the 'EXit' command.

REname Source Destination

Changes the name of the plot object specified by the pathname 'Source' to the plot object specified by the pathname 'Destination'. Same action as the 'MV' (MoVe) command.

RM Pathname ...

This command removes the plot object(s) specified on the command line. The plot object(s) specified should exist before deletion. Same action as the 'DElete' command.

SHA Granularity Source Dest

Creates in the file specified by the pathname 'Dest' a Mentor Charting Utility File of Oxide Area vs. Stress for the stress information in the file specified by the pathname 'Source'. 'Granularity' specifies the increment

of stress factor that the analysis will use.

SHEll <Command ... >

This creates an Aegis Shell by means of /com/sh. The Oxide Stress Analyzer will remain intact, but you will be able to make full use of Aegis until you quit the shell with a Control-Z (this will cause '*** EOF ***' to be printed, and you should be returned to the 'OSA>' prompt). If '<Command ... >' is specified, the shell will attempt to execute it just as if it were entered to an Aegis Shell, and you will be returned to the Oxide Stress Analyzer automatically upon completion of '<Command ... >'.

SHOw Pathname ...

This command displays contents of the plot object(s) specified on the command line.

Unlock Patnname ...

Removes a lock from the plot object(s) specified by the pathnames. This restores the ability to plot, edit, or delete (see the 'PLot', 'EDit', 'DElete', and 'RM' commands) the specified object(s). See 'LOck' for a description of placing a lock on a plot object or group of objects.

Wd <Pathname>

Set the current working directory. This is similar to the Aegis "Working Directory" Command. See the System Help directory for details (type HELP WD to a shell).

!<Command>

Repeat a command. <Command> can be a number, a sequence of alphanumerics, or a '!' character. If it is a number, the command matching that location in the history will be executed. For example, !4 will execute the fourth command in the history, if it exists. If <Command> is a sequence of alphanumerics (no leading digits), a command in the history that begins with the specified characters will be searched for and executed. For example, if the fourth command in the history was 'ld -a -nhd' and the fifth command in the history was 'ld', then '!l' would execute the fifth command ('ld'), and '!ld -' would execute the fourth command ('ld -a -nhd'). If <Command> is '!', the last command entered will be executed. Note that <Command> must immediately follow the '!'.

B. Data Acquisition Environment Help File

Title: Data Acquisition Environment (DAE)

Author: James M. Roucis

Date: 8-8-88

Location: Martin Marietta, Astronautics Group

The following is a concise list of DAE commands and their syntax. The definitions of these commands are given in this format:

Command Name Command Token

Command line format

Description

Example(s)

The form <token> indicates that a sequence of characters referenced by the word 'token' in the description is REQUIRED in the syntax of a give command. The form [token] indicates that a sequence of characters referenced by the word 'token' in the description is OPTIONAL in the syntax of a give command. Elipses (i.e. '...') indicate one or more items.

ASSIGN =

= $<identifier> <expression>

This command assigns a value to a variable. The name of the variable is specified by the <identifier> field. This name may be no more than 31 characters long and must be preceeded by the '$' shown above. It is safest to use only alpha characters in a name. If a variable is specified that has not been specified before, it is created and the value of <expression> will be assigned to it. Otherwise, an existing variable will simply take on the value of <expression>. The form for <expression> is as follows:

<operator> [arguments ...]

<operator> and [arguments ...] may be one of the following:

? [prompt string ...]

This operator allows a string of characters to be assigned to a variable. If [prompt string ...] is not specified, a default prompt will be given. The prompt string begins at the first non-whitespace character after the '?' operator, and ends just before the carriage return at the end of the line.

+ <arg1> [arg2] [arg3] [arg4] [arg5] [arg6] [arg7] [arg8]

This operator returns the sum of its arguments. An argument may be an INTEGER in the range -2147483648 to +2147483648 or the identifier of an existing variable.

- <arg1> [arg2] [arg3] [arg4] [arg5] [arg6] [arg7] [arg8]

This operator returns the result of subtracting the remaining arguments from its first argument. An argument may be an INTEGER in the range -2147483648 to +2147483648 or the identifier of an existing variable.

* <arg1> [arg2] [arg3] [arg4] [arg5] [arg6] [arg7] [arg8]

This operator returns the product of its arguments. An argument may be an INTEGER in the range -2147483648 to +2147483648 or the identifier of an existing variable.

/ <arg1> [arg2] [arg3] [arg4] [arg5] [arg6] [arg7] [arg8]

This operator returns the result of dividing the first argument by the remaining arguments. An argument may be an INTEGER in the range -2147483648 to +2147483648 (excluding zero) or the identifier of an existing variable.

Variables are global. That is, any variable, once defined, may be referenced from within any macro file or from the interactive shell. There is a limit of 128 variables for a given invocation of the DAE.

Examples:

= $filename ? Please enter the name of a file:

= $sum + 1000 $base 23

EXECUTE @

@ <filename> [arguments ...]

This command causes the DAE to execute a sequence of commands stored in a text file whose pathname is given by <filename>. <filename> may be an explicit string or a variable, but in either case it must be a valid pathname.

If specified, [arguments ...] should be either explicit strings or variables. These strings or values of variables will be passed to the command file (or "macro file") and may be referenced in the file by the identifiers $0 through $9. Identifier $0 contains the name of the macro file itself, and $1 through $9 reference the arguments given to the macro file on the command line. This implies that only 9 arguments may be passed to a macro file.

Commands in the file will be executed in sequence until an error occurs or all command lines are exhausted. Other macro files may be executed from within a macro file, but the nesting level is controlled by the configuration of the host computer. The level SHOULD be greater than 8.

Upon entering a macro file, no GPIB device will be addressed. Upon exiting a macro file, any GPIB device that had been addressed before execution will again be the currently addressed device.

Examples:

```
@ initdev1

@ moveby 100 20

@ dumprslt $filename $date $time
```

LOOP &

& <count> <filename> [arguments ...]

This command enables repeated execution of a macro file specified by <filename>. The <count> field should specify an integer number of times to execute the macro file. It should be a quantity in the range 1 to +2147483648. [arguments ...] should be as described in the EXECUTE command.

Examples:

```
& 10 /scope/getdata

& 4 /prober/step 100 0
```

```
    & $count $rampto $limit
```

OPEN [

```
[ <GPIB device>
```

This command attempts to address a device on the local GPIB. The <GPIB device> field should contain a string or a variable whose value identifies a valid device. See the National Instruments manual to learn how to define devices on the local GPIB.

If this command executes properly, subsequent DAE commands that communicate with GPIB devices (see READ and WRITE for examples) will address this device specified. This will be the case until another OPEN is successfully executed for another device. Upon initial invocation of the DAE, no device will be addressed.

Examples:

```
[ scope1

[ $device
```

OUTPUT %

```
% [+]<destination> [text ...]
```

This command writes text to a place specified by <destination>. This field should be an explicit file name, a variable whose value is a valid file name, or the character '*'. If the <destination> evaluates to a file name, then a file is opened, and the characters in the [text ...] field will be placed in it. If this file name is preceeded by a '+' character, then the [text ...] field will be APPENDED to the specified file. If the '*' character is given, the [text ...] field will be written to the screen. The [text ...] field should be any combination of literal strings and variables.

Examples:

```
% /prober/username Current user of the probe station is D. Krening.

% /prober/date Today's date is $date.

% +$datefile The time is $time.
```

```
% * Welcome to the Data Acquisition Environment.
```

PAUSE *

```
* [message ...]
```

This command allows a macro file to pause execution until the user strikes a key. The [message ...] field specifies a prompt for the user explaining the pause. If not specified, a default message will be given.

Examples:

```
*

* Please configure $device1 and strike a key to continue...
```

POLL :

```
:
```

This command conducts a GPIB "serial poll" and returns the results. See the National Instruments GPIB manual for a description of the significance of a "serial poll". A device must be currently addressed on the GPIB.

Examples:

```
:
```

QUERY ?

```
? <true macro file> <false macro file> [prompt ...]
```

This command provides for conditional execution of macro files. The user is prompted to give a 'Y' or 'N' response to a question. If the user answers with a 'Y', the macro file specified by the <true macro file> field will be executed. If the user answers with an 'N', the macro file specified by the <false macro file> field will be executed. If the [prompt ...] field contains strings and/or variables, they will be used to prompt the user for an answer. Otherwise, a default prompt will be given.

Examples:

```
? /prober/getdata /prober/exit Get more data?

? $init $continue Initialize the equipment again?
```

QUIT q ^Z

```
q

^Z
```

This command causes the DAE to exit. If it is encountered in a macro file, the user will be asked if the DAE should quit or continue. If the user chooses to quit, the DAE halts. Otherwise, the macro file containing the QUIT command will be exited immediately; any commands in the file following the QUIT command will be ignored.

Examples:

```
q

^Z
```

RAMP /

```
/
```

This is a special command. This command causes the device called VSRC1 to output a single ramp voltage. See the WAVEFORM command description for an explanation of creating ramp signals. This command temporarily addresses the VSRC1 device, restoring any previously addressed device after completion.

Examples:

```
/
```

READ <

```
< [+][filename]
```

This command reads data from the currently addressed device on the GPIB. A device must be addressed. If the [filename] contains a valid file name or a variable whose value is a valid file name, the results of the read will be written to the specified file. If the file name

is preceeded by a '+' character, the results of the read will be APPENDED to the given file. If no file name is specified, the results of the read will be printed directly to the screen.

Examples:

```
<

< +/prober/results

< $results
```

REPEAT

This is a special command. This command repeatedly causes the device called VSRC1 to output a ramp voltage. See the WAVEFORM command description for an explanation of creating ramp signals. This command temporarily addresses the VSRC1 device, restoring any previously addressed device after completion.

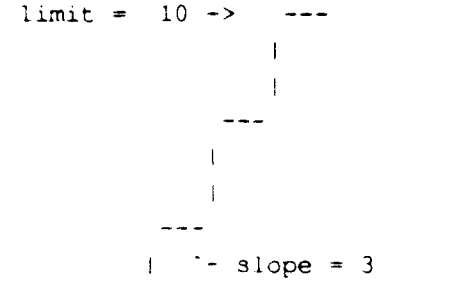
Examples:

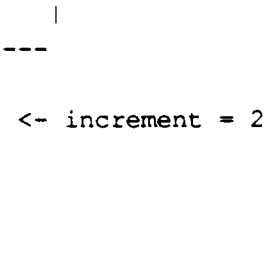
WAVEFORM

```
 <limit> <increment> <slope>

 ['<' | '>']<filename>
```

This command provides for constructing, saving, or recalling a waveform description for a Kepco BOP50-2M voltage source. In the command's first form, the <limit>, <increment>, and <slope> fields define the waveform in the following manner:





The second form of the command allows a waveform to be written to or read from a file. The file is specified by <filename> and the direction of the operation is specified by the leading '<' or '>' character. A '<' indicates that a waveform is to be read from the file while a '>' indicates that the current wavefrom is to be written to the specified file.

Examples:

- 3000 10 2
- $limit $increment $slope
- <wavefrm.1
- >$waveout

WRITE >

> <message>

This command writes the characters contained in <message> to the currently addressed device on the GPIB. A device must be addressed. The message sent to the device starts with the first non-blank character after the '>' and ends at the end of the line.

Examples:

> INIT

> $message

```
;
;  Move the probe station's stage by the amounts specified by the
;  macro file arguments --
;

;
; Parameter 1: $1 - Jog size in X direction
; Parmeter  2: $2 - Jog size in Y direction
;

[ prober1
  >  XM$1,YM$2,R,DP
  <  MUNGFILE



;
; DAE driver file to initialize test of PWELL capacitors
;   with a ramp voltage.
;

;
; Initialize the voltage source
;
[ VSRC1
  ; Make sure the output voltage is zero
  > 000000
  ;  Set up the voltage ramp
  ;     ~ 4000 1 1
  ~ <w400011.wav

;
; Initialize the scope using a stored setting
;
[ SCOPE1
  > RECALL FPS3

;
; Initialize the probe station
;
[ PROBER1
  * Clear the platen area (Hit any key when ready...)
  > J0,EP1,DM
  < MUNGFILE
  > UP,H
```

```
;
; DAE driver file to blow one PWELL capacitor
;

;
; Parameter 1: $1 - Capacitor sequence number
; Parmeter  2: $2 - Capacitor size code
; Parmeter  3: $3 - Data file

;
; Arm the scope for a single acquisition
;
[ SCOPE1
  > CONDACQ TYPE:SINGLE
  < MUNGFILE

;
; Blow the cap
;
[ VSRC1
  /

;
; Get data from scope and write to file
;
[ SCOPE1
  % +$3 NAME "$1 $2"
  > OUTPUT TRACE1
  > WAVFRM?
  < +$3




;
; DAE file to test a row of PWELL capacitors
;   with a ramp voltage
;

;
; Set the capacitor spacing
;
= $spacing 200
= $xincr   0
= $yincr   - 0 $spacing
```

```
;
; Prompt user to position wafer to 1st capacitor
;
[ PROBER1
  > J0,EP1,DM
  < MUNGFILE
  > UP
  > J1,DM
  < MUNGFILE
  * Position the wafer to the 1st capacitor (and set probes...)
  ;
  ; Regain control of probe station and set some parameters
  ;
  ;   Get control, set units to microns, and set present position to zero
  > J0,U1,Z,DP
  < MUNGFILE
  ;   Enable platen.
  > EP1,DM
  < MUNGFILE

;
; Blow the capacitors
;
;   Get capacitor identifiers
= $wafer ? Enter Wafer ID Number (e.g. W1)       >
= $site  ? Enter Reticle Site Number (e.g. R14) >
= $type  ? Enter Capacitor Type (PWELL | SUBS)  >
;   Construct file name for this capacitor data
= $file  ? Enter File Name (e.g. W1R14.PW)       >
;   Write file header (date, filename, and time...)
[ SCOPE1
  % $file FILE "$file"
  > DATE?
  < +$file
  > TIME?
  < +$file
  % +$file ID "$type $wafer $site"
  % +$file TTYPE "RAMP"
  % +$file TTEMP "27.0"

;   Get the ramp waveform
[ SCOPE1
  > TRACE1 DESCRIPTION:"L1"
  > CONDACQ TYPE:SINGLE
  < MUNGFILE
;   Make sure platen is up
[ PROBER1
```

```
  > UP
  < MUNGFILE
;   Generate the ramp voltage
[ VSRC1
  /
[ SCOPE1
  % +$file NAME "RAMP"
  > OUTPUT TRACE1
  > WAVEFORM?
  < +$file
  > REMOVE TRACE1
;   Set up scope for capacitor data capture
[ SCOPE1
  > TRACE1 DESCRIPTION:"L2"
  > TRMAIN SOURCE:"L1"
  < MUNGFILE
;   Make sure platen is down
[ PROBER1
  > DN
;   Blow the capacitors
@ PWBLOW1 1 B $file
@ RMOVE -200 0
@ PWBLOW1 2 A $file
@ RMOVE -200 0
@ PWBLOW1 3 B $file
@ RMOVE -200 0
@ PWBLOW1 4 A $file
@ RMOVE -200 0
@ PWBLOW1 5 C $file
@ RMOVE -200 0
@ PWBLOW1 6 C $file
@ RMOVE -200 0
@ PWBLOW1 7 B $file
@ RMOVE -200 0
@ PWBLOW1 8 A $file
@ RMOVE -200 0
@ PWBLOW1 9 B $file
@ RMOVE -200 0
@ PWBLOW1 10 A $file
@ RMOVE -200 0
@ PWBLOW1 11 C $file
@ RMOVE -200 0
@ PWBLOW1 12 C $file
;& 15 PWBLOW
```

C. Test Vehicle Detailed Schematics

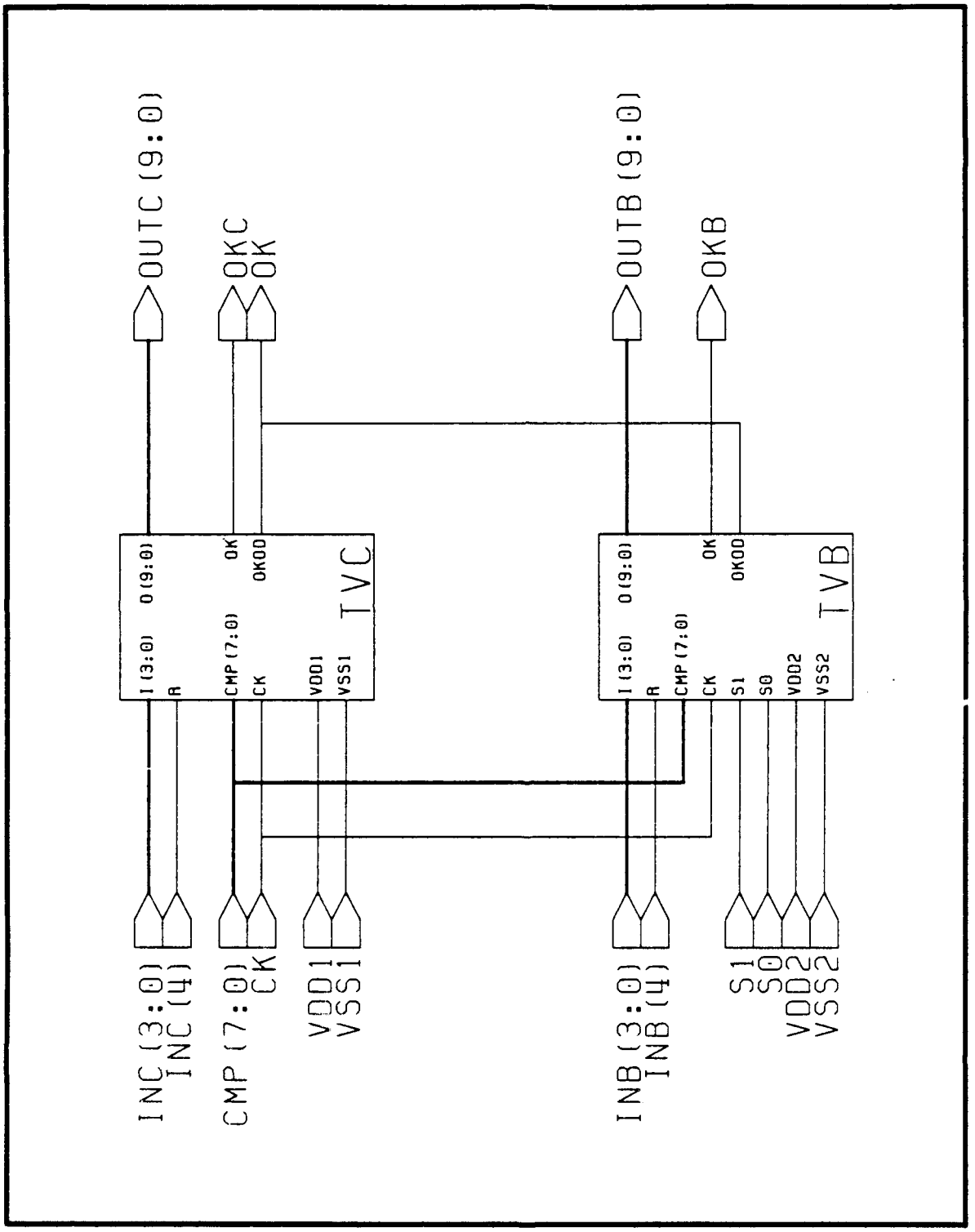


Figure 79 RLOS Test Vehicle Top Level

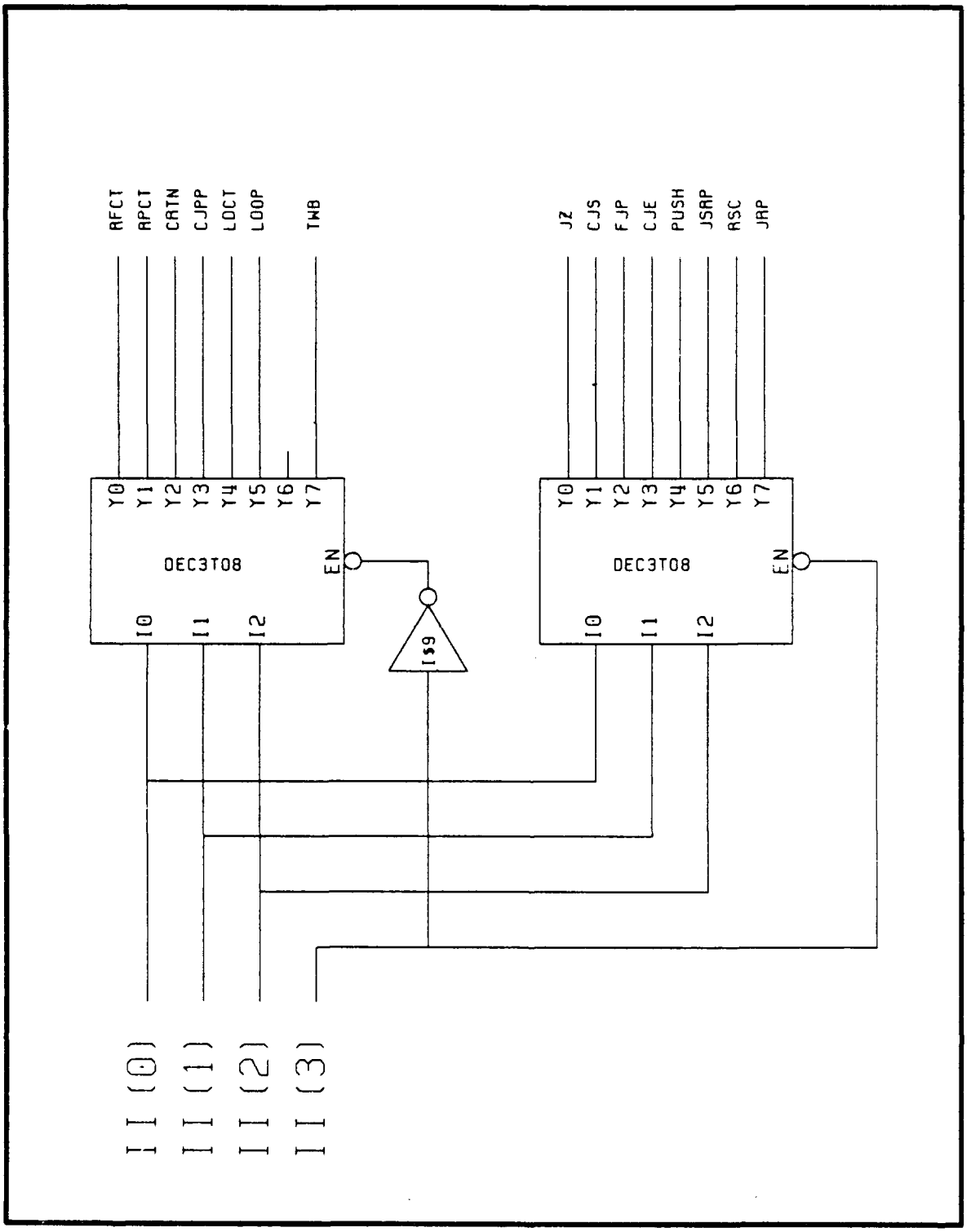


Figure 80 RLOS Test Vehicle (B,C) Sheet 1

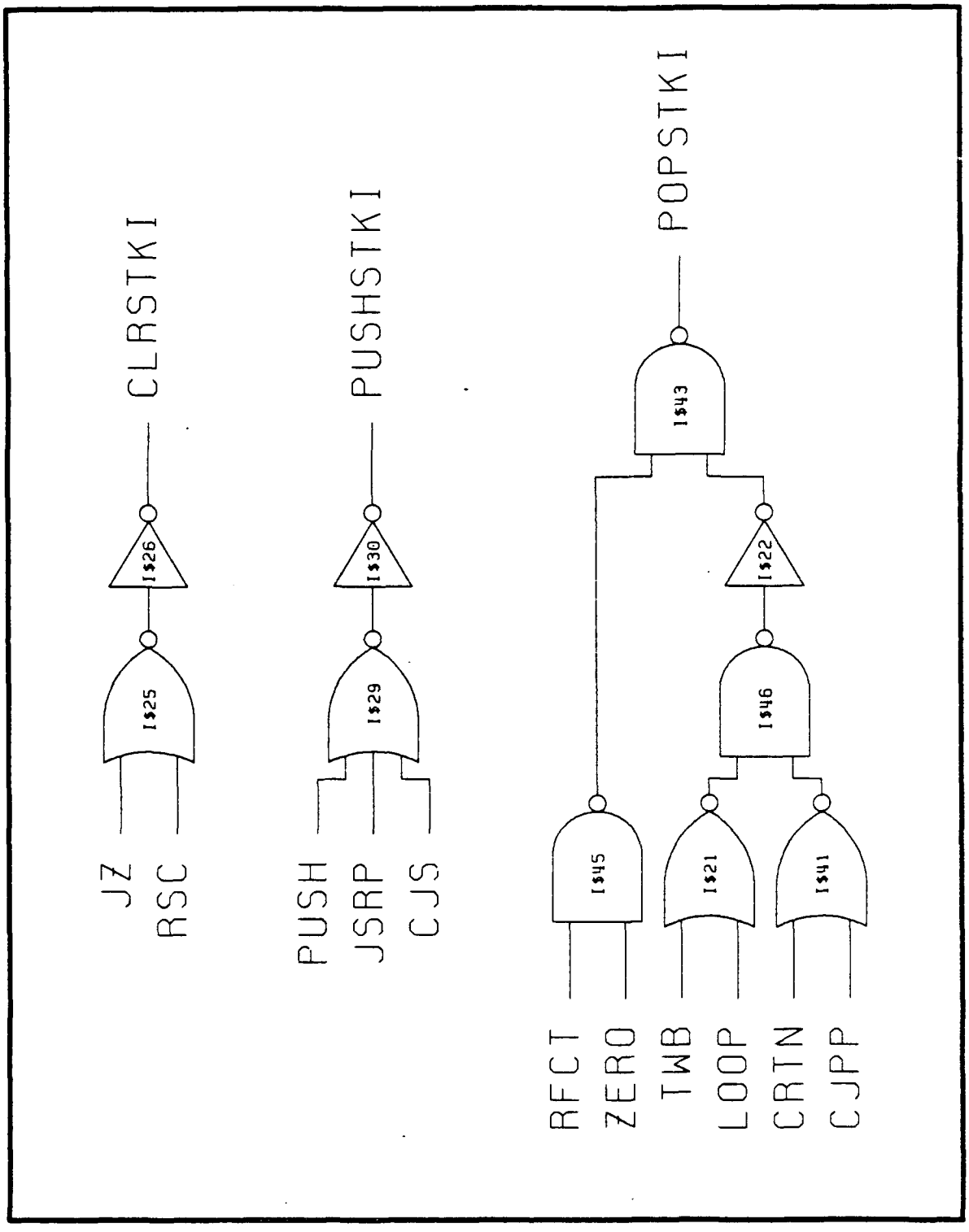


Figure 81 RLOS Test Vehicle (B,C) Sheet 2

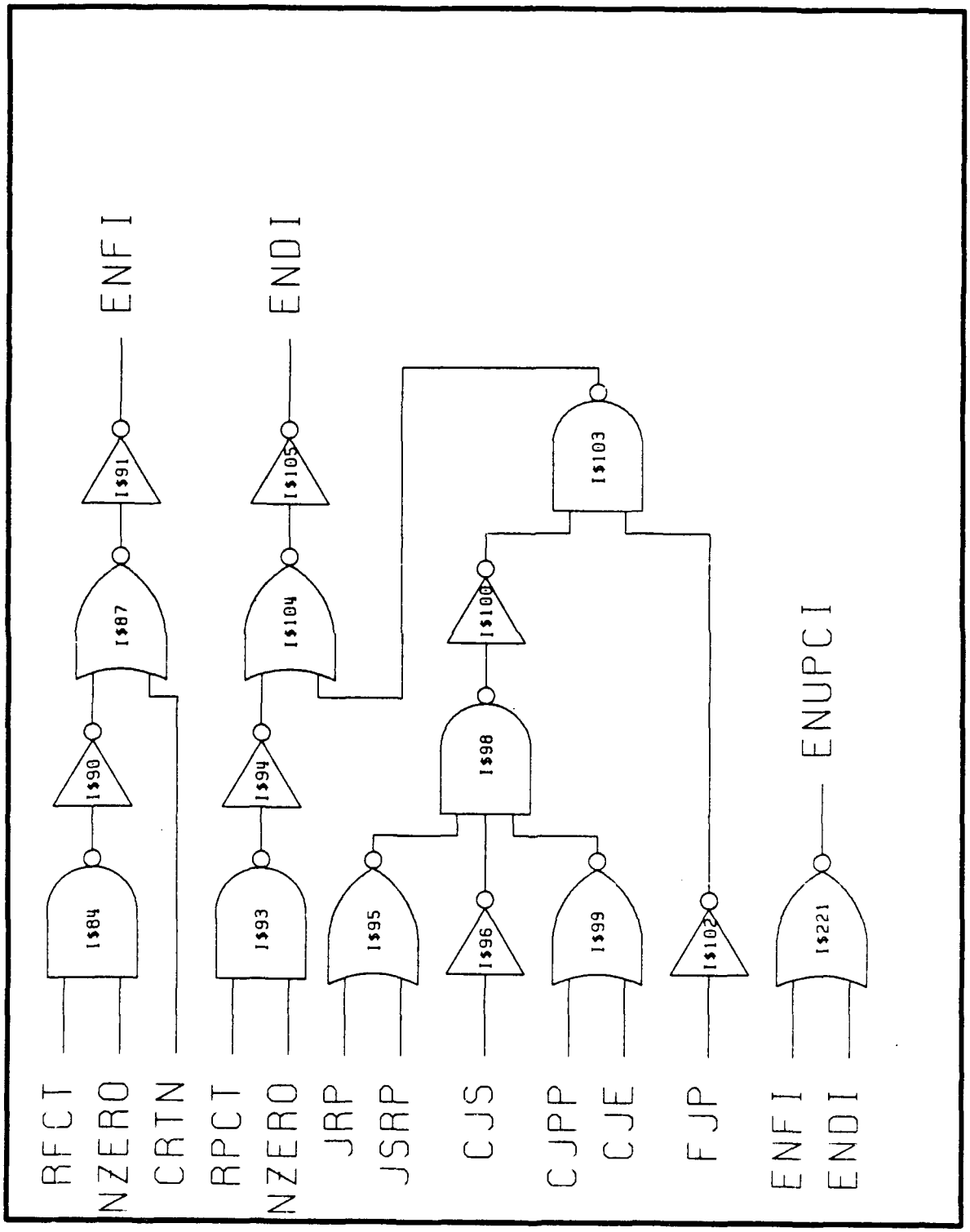


Figure 82 RLOS Test Vehicle (B,C) Sheet 3

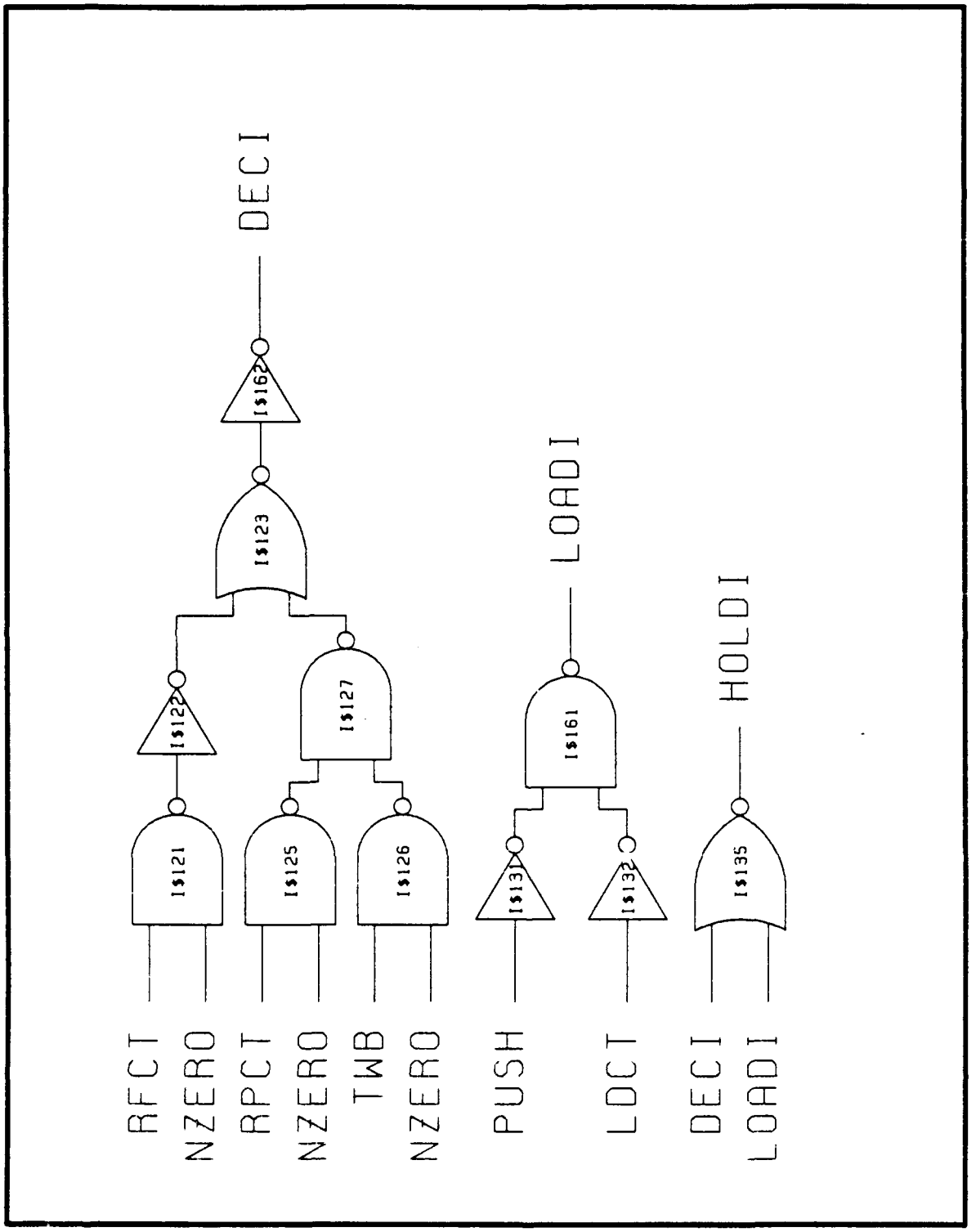


Figure 83 RLOS Test Vehicle (B,C) Sheet 4

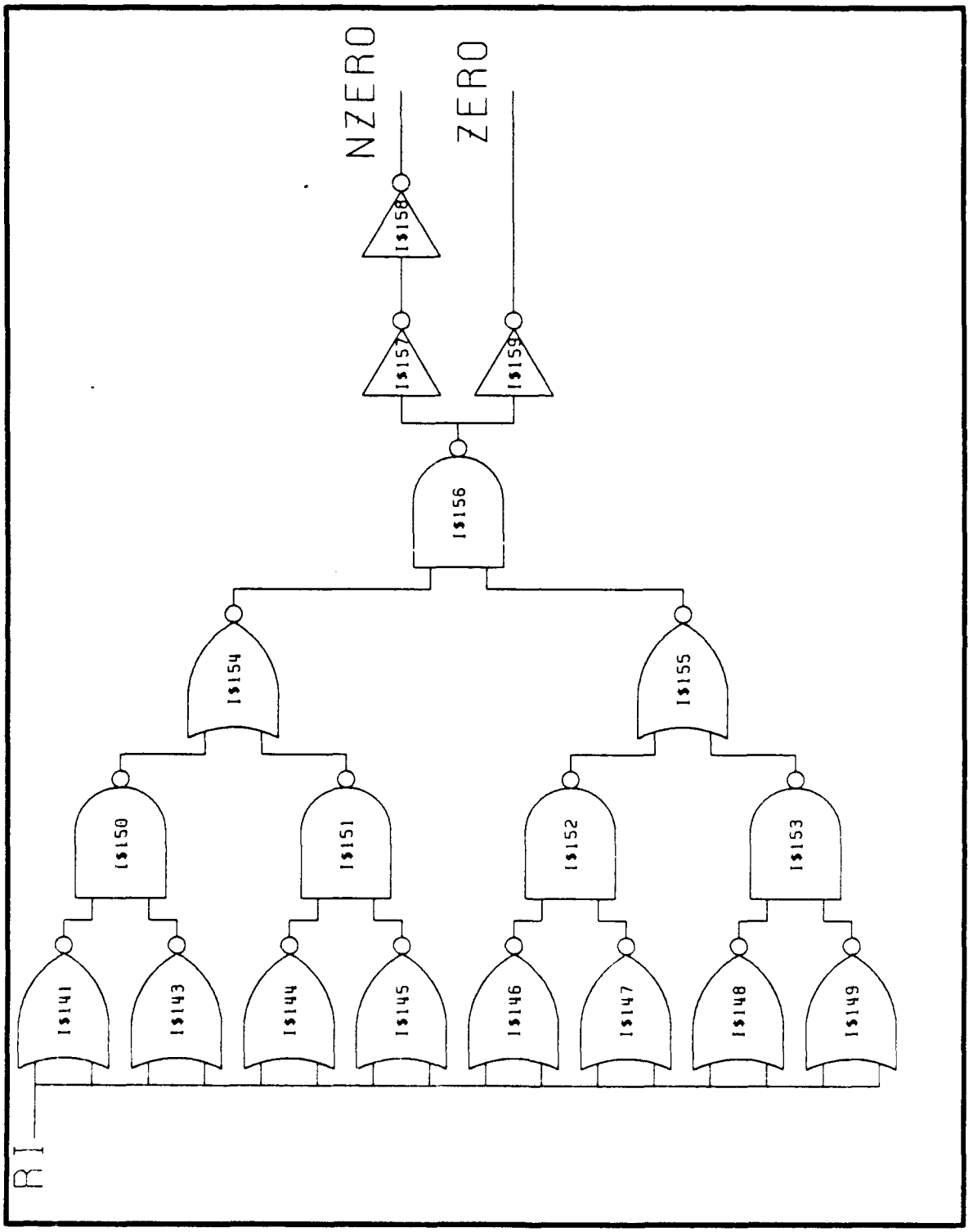


Figure 84 RLOS Test Vehicle (B,C) Sheet 5

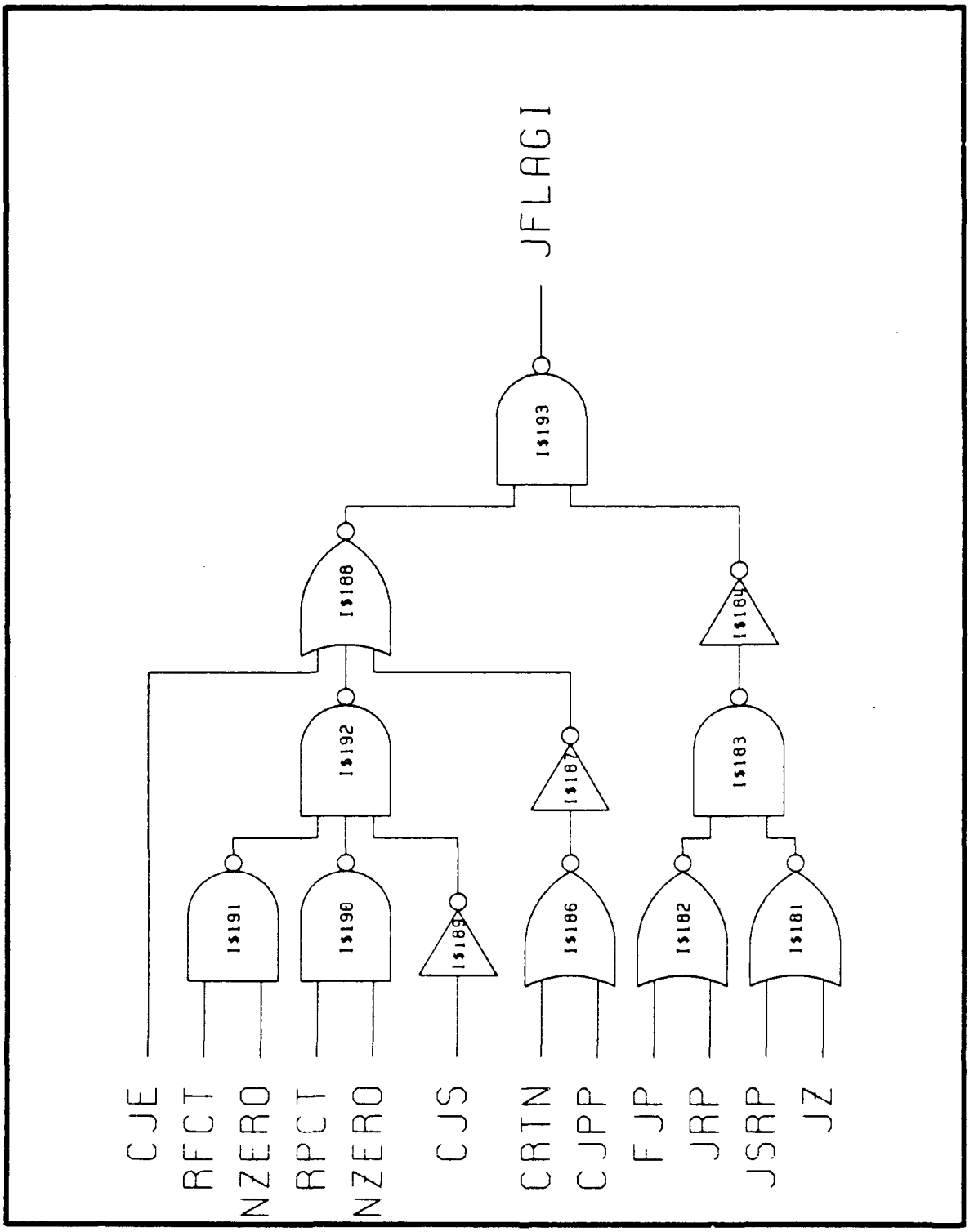


Figure 85 RLOS Test Vehicle (B,C) Sheet 6

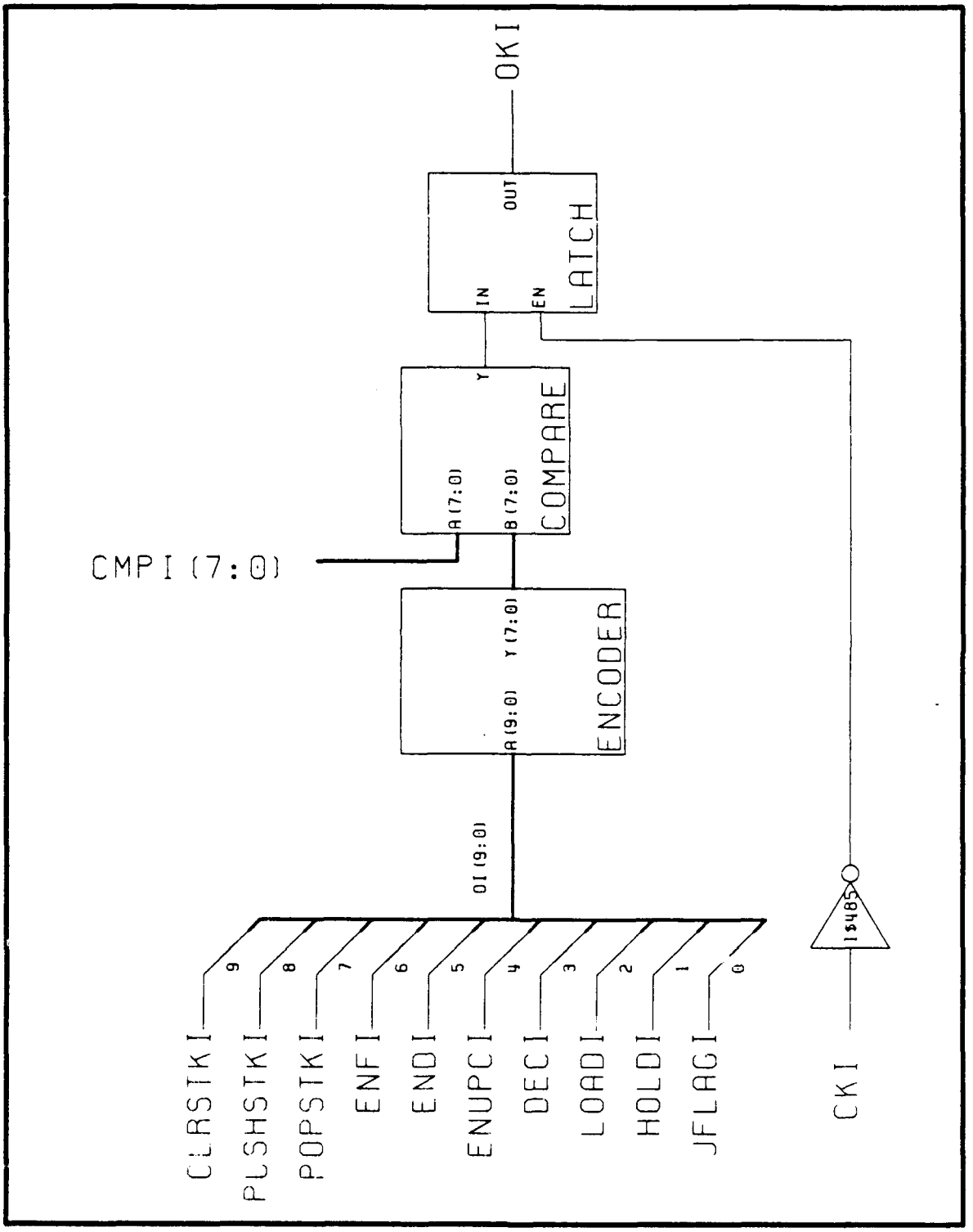


Figure 86 RLOS Test Vehicle (B,C) Sheet 7

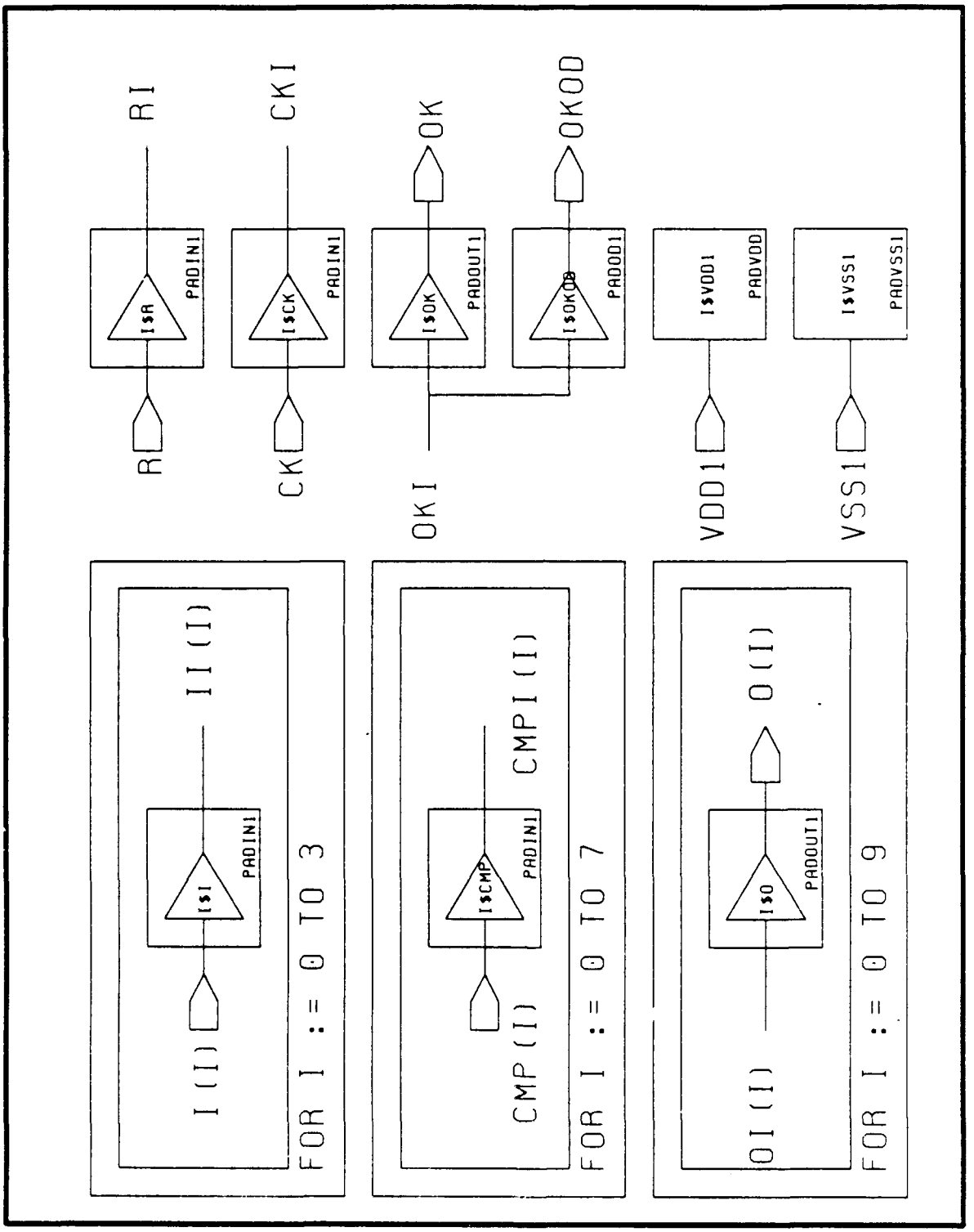


Figure 87 RLOS Test Vehicle (B,C) Sheet 8

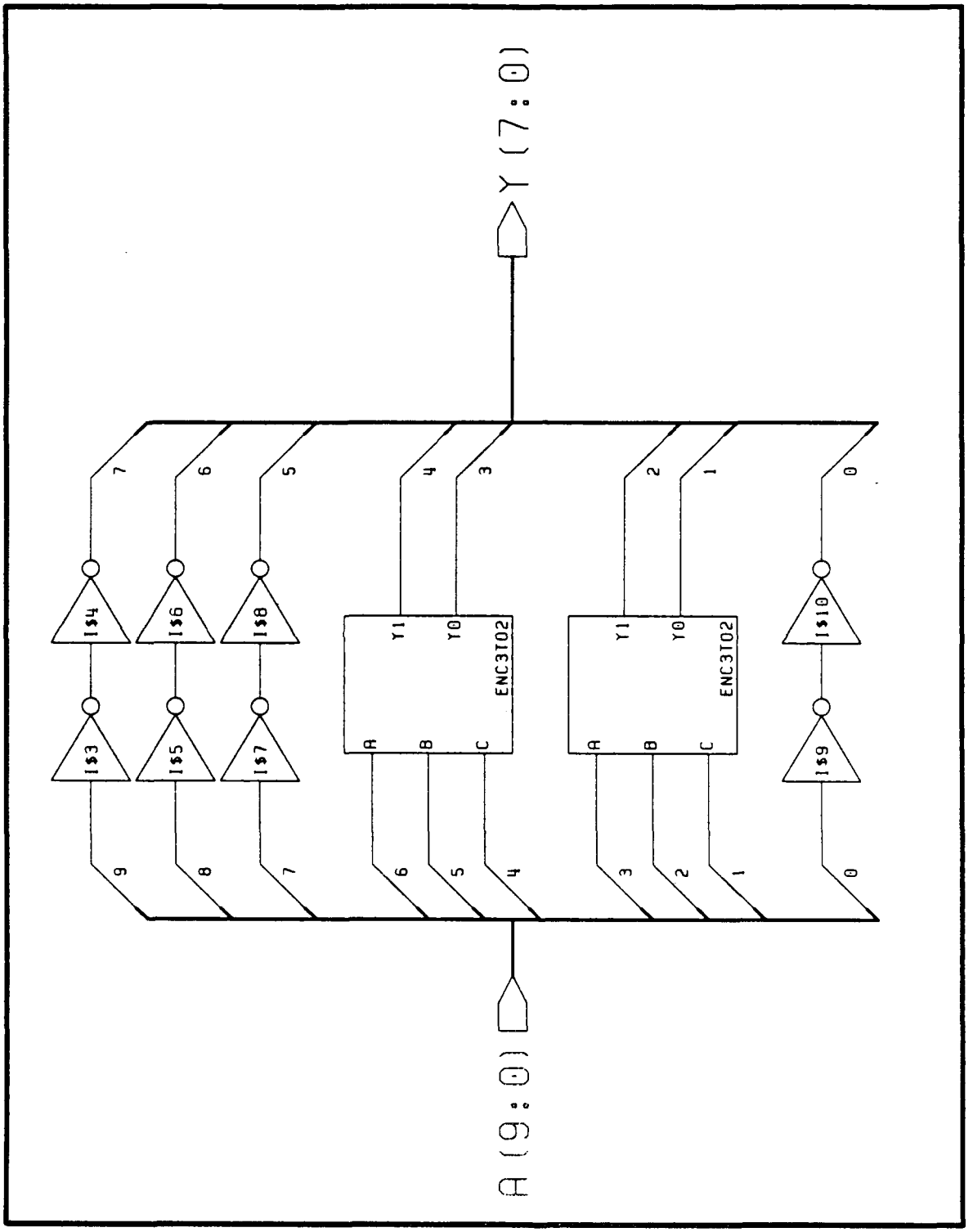


Figure 88 RLOS Test Vehicle (B,C) Encoder

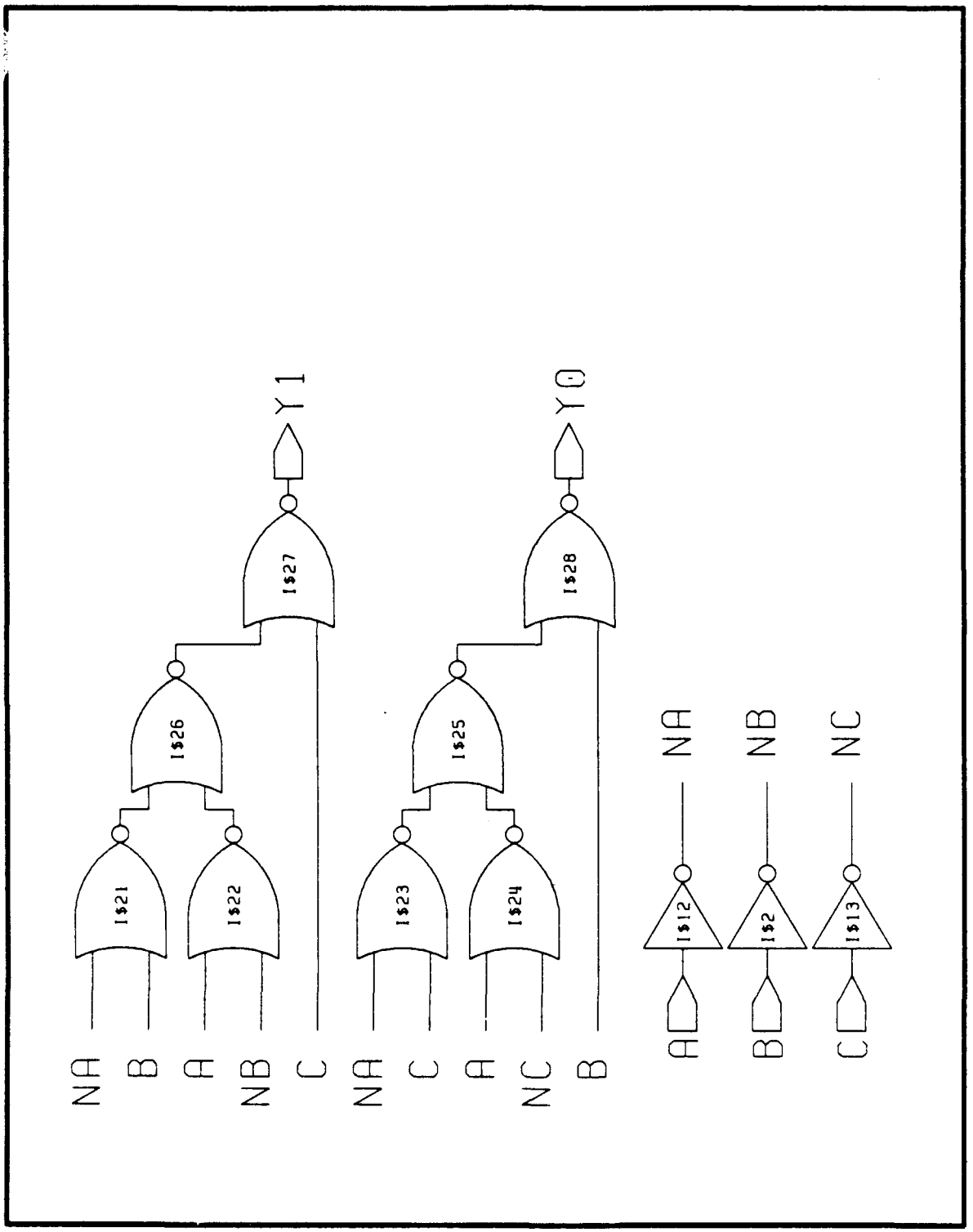


Figure 89 RLOS Test Vehicle (B,C) 3-to-2 Encoder

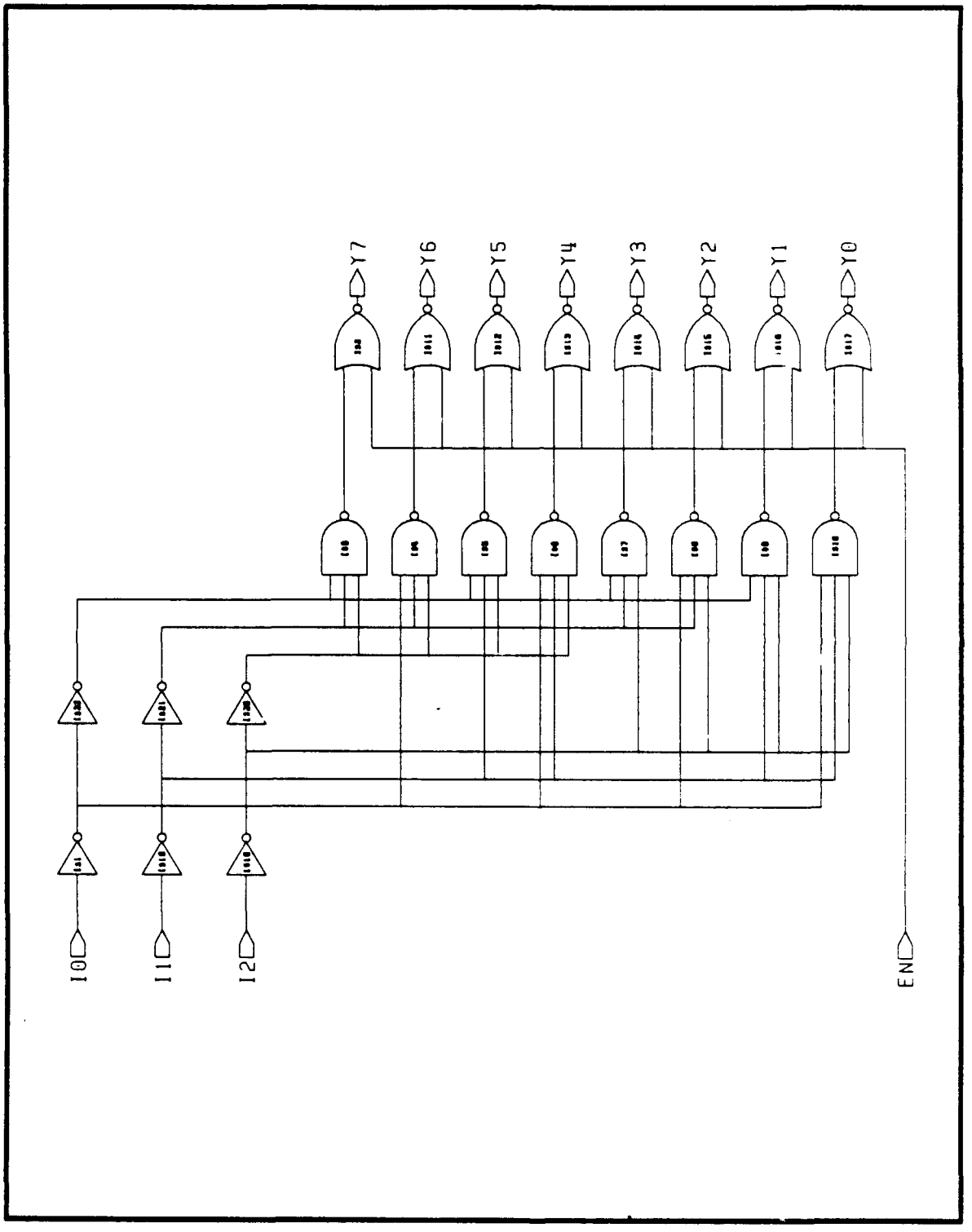


Figure 90 RLOS Test Vehicle (B,C) 3-to-8 Decoder

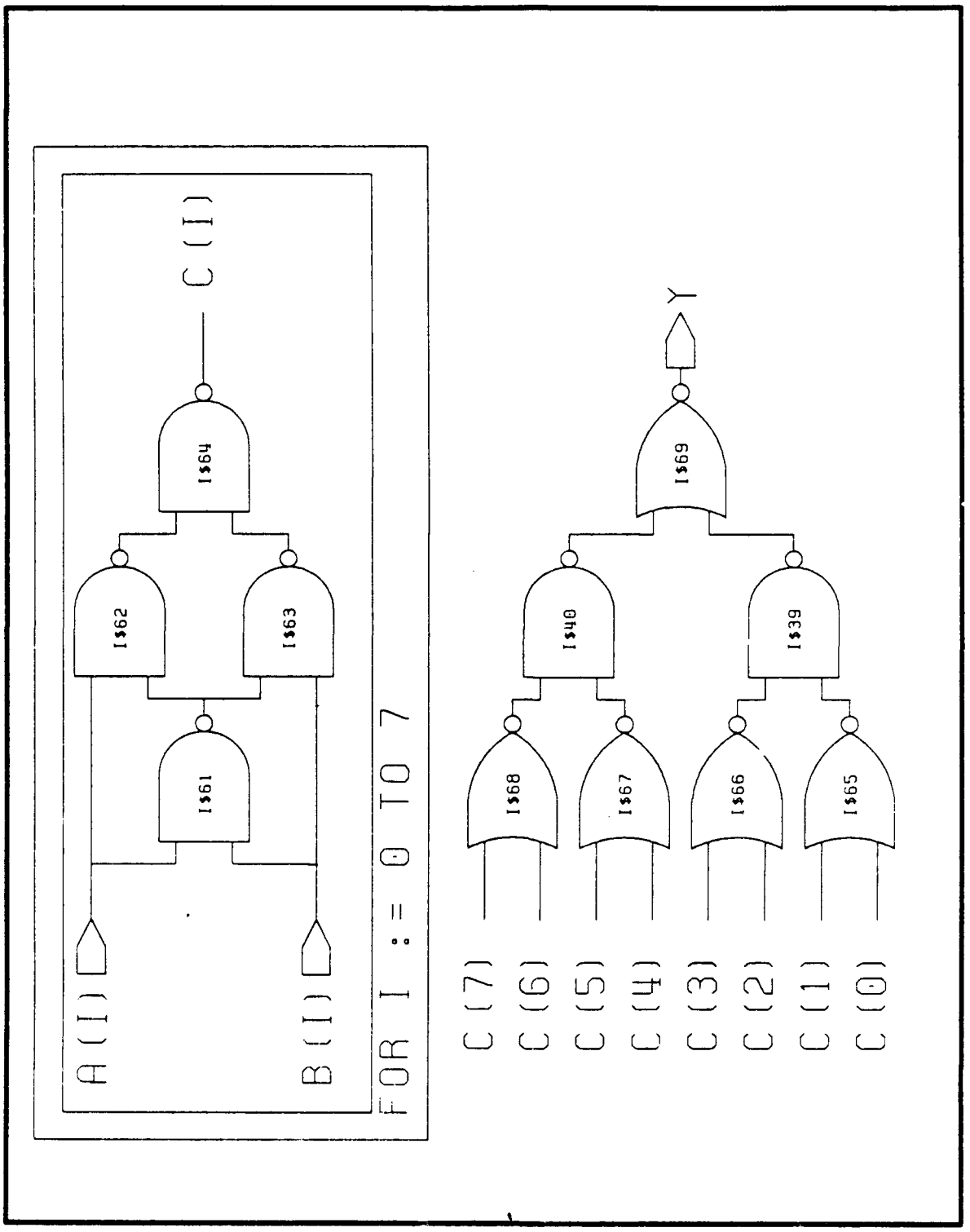


Figure 91 RLOS Test Vehicle (B,C) Comparator

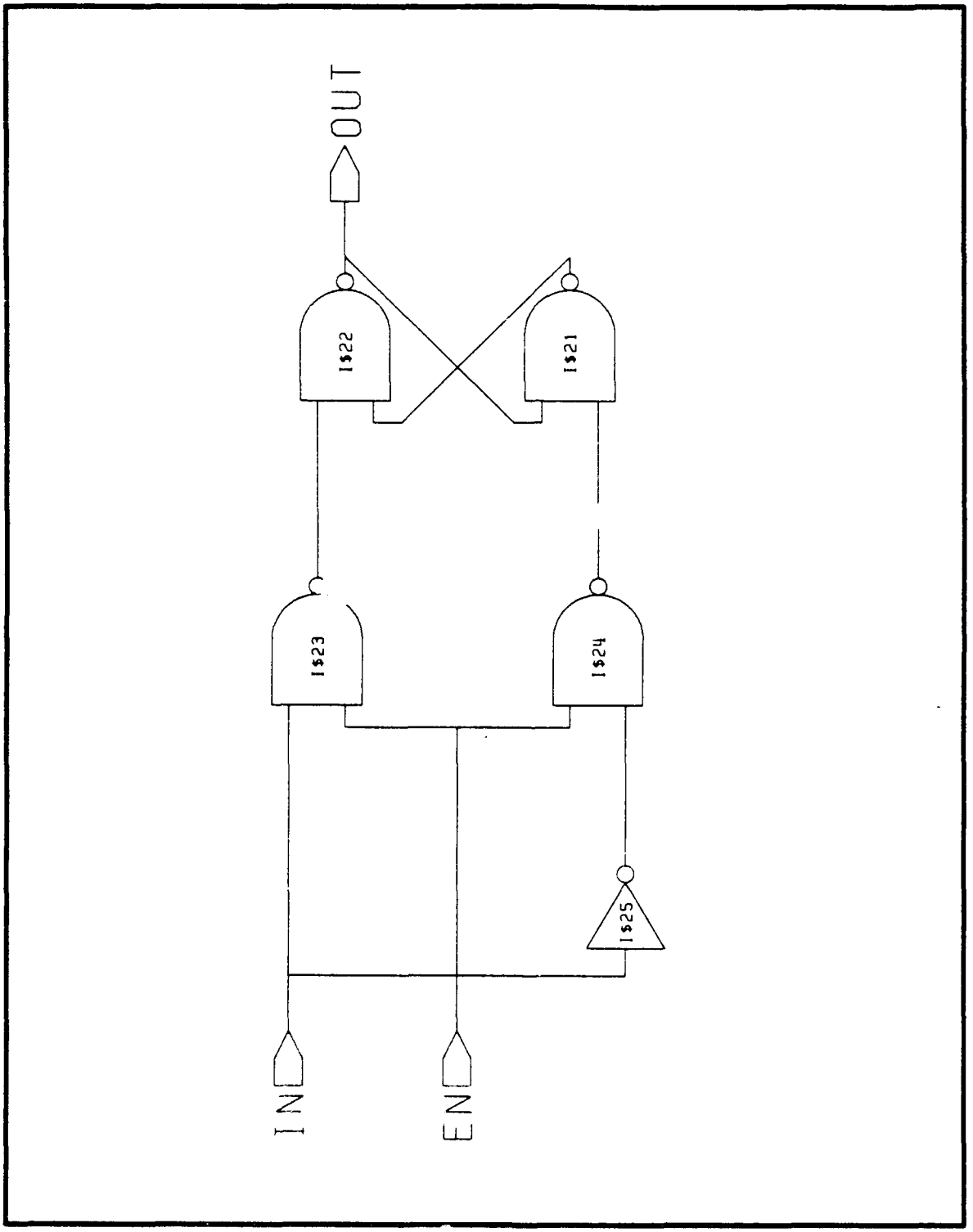


Figure 92 RLOS Test Vehicle (B,C) Latch

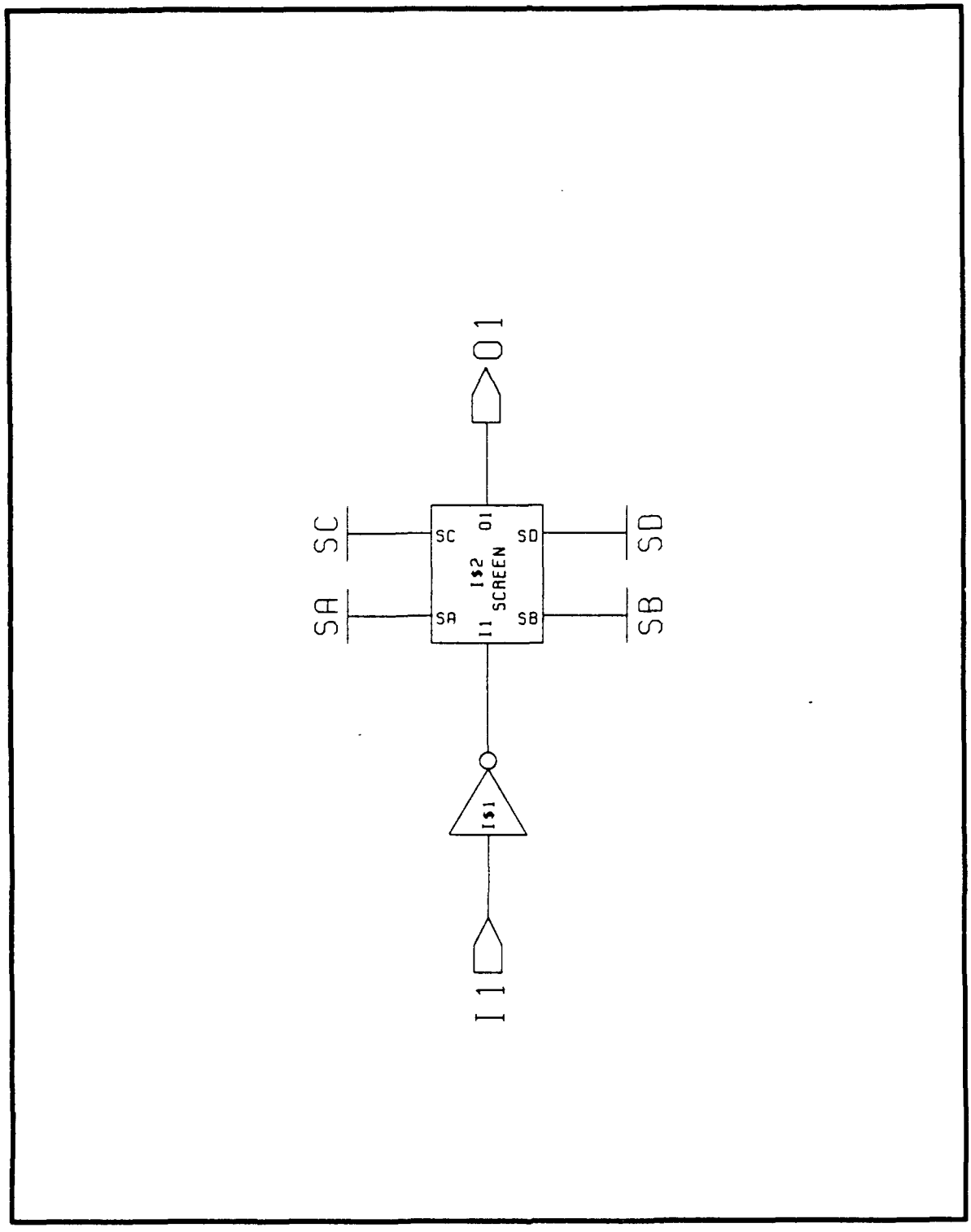


Figure 93 RLOS Test Vehicle B Inverter with Stress

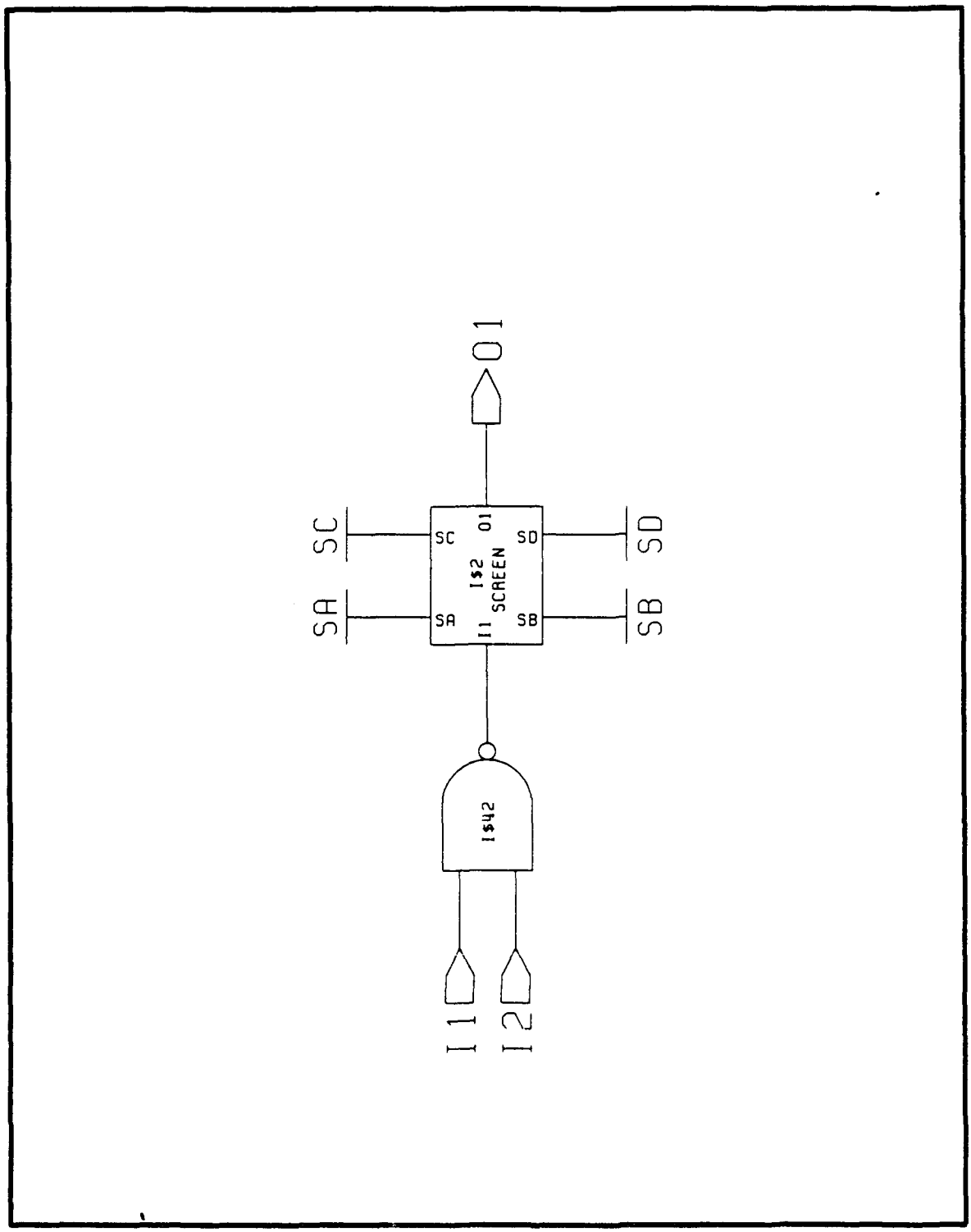


Figure 94 RLOS Test Vehicle B 2-Input NAND with Stress

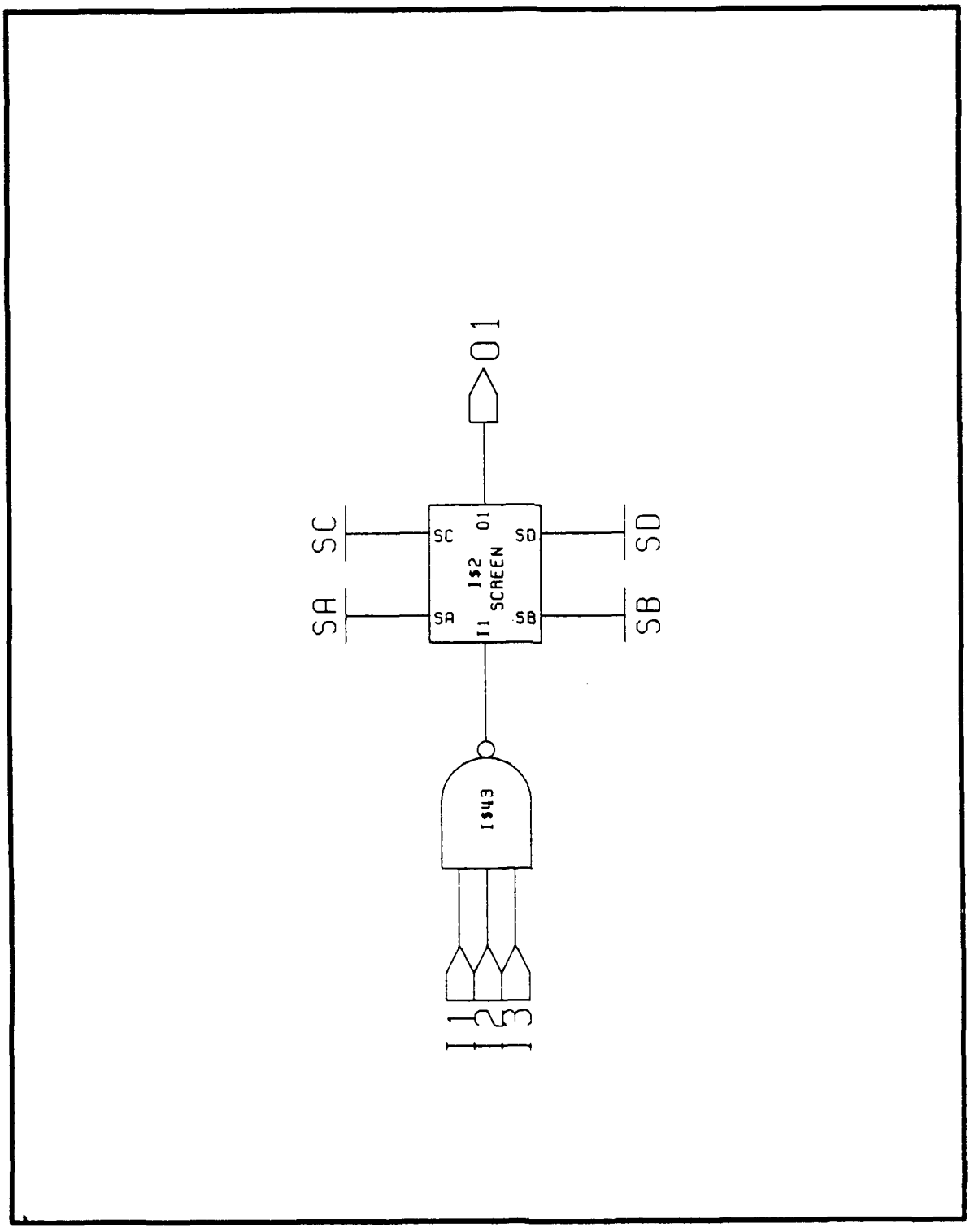


Figure 95 RLOS Test Vehicle B 3-Input NAND with Stress

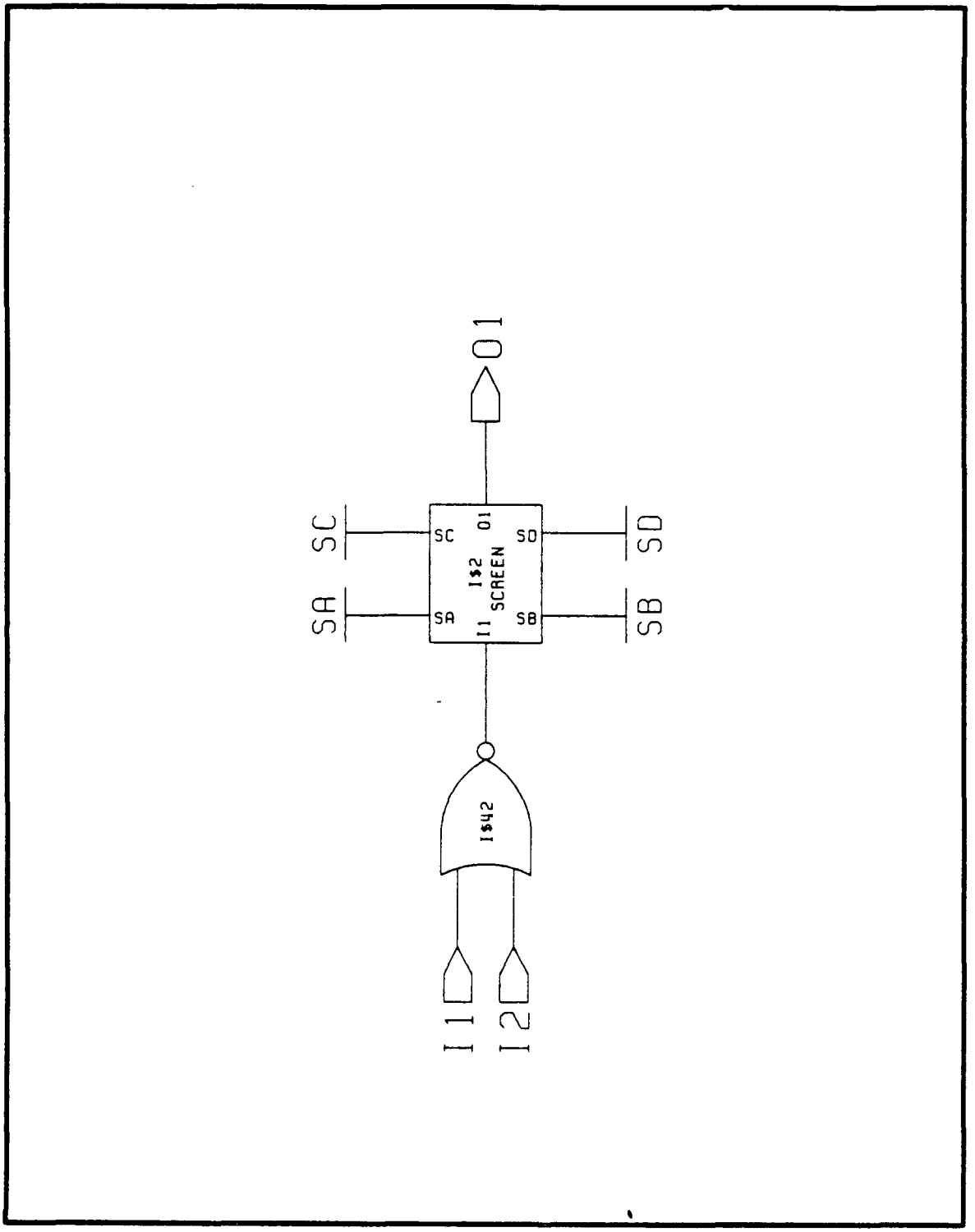


Figure 96 RLOS Test Vehicle B 2-Input NOR with Stress

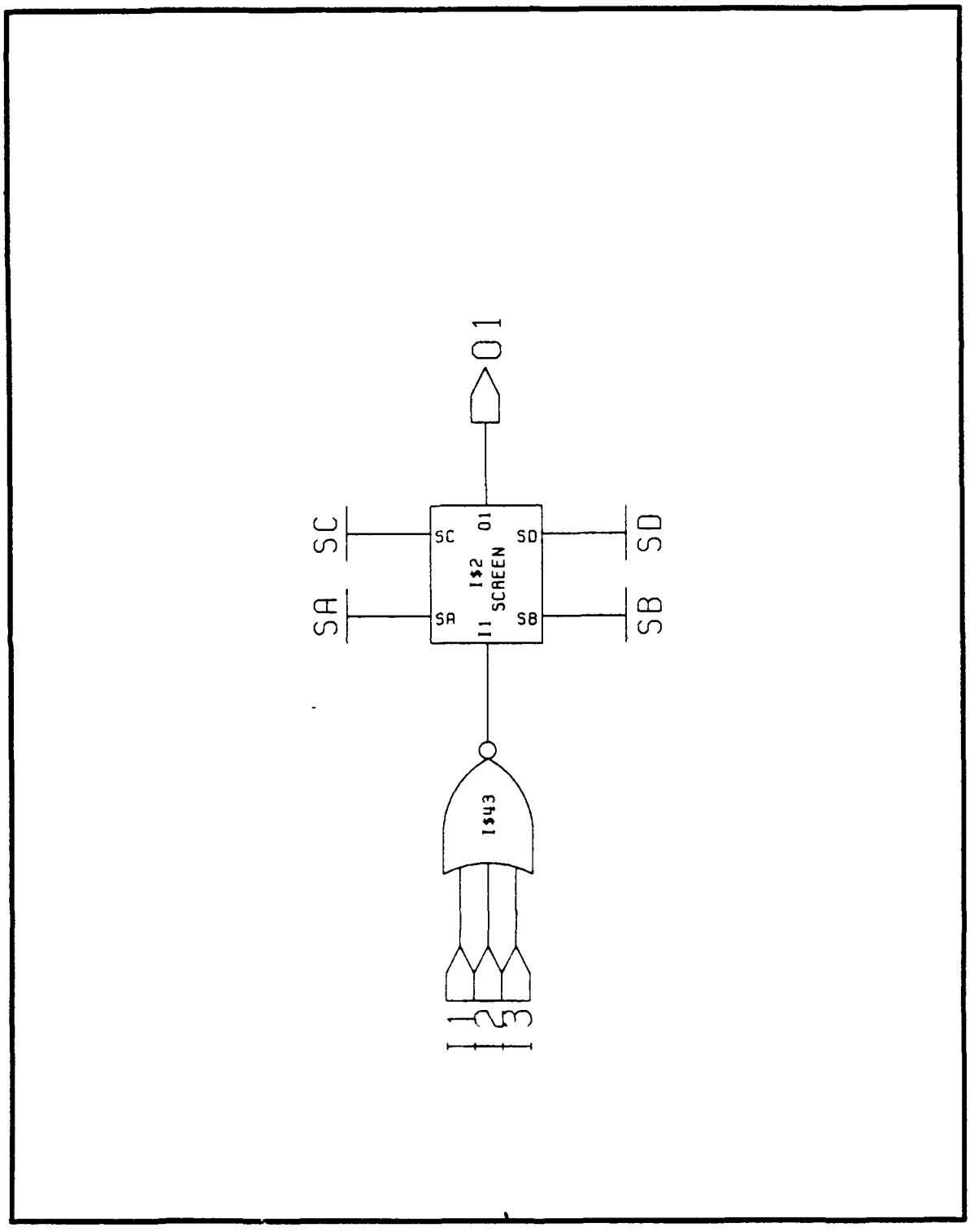


Figure 97 RLOS Test Vehicle B 3-Input NOR with Stress

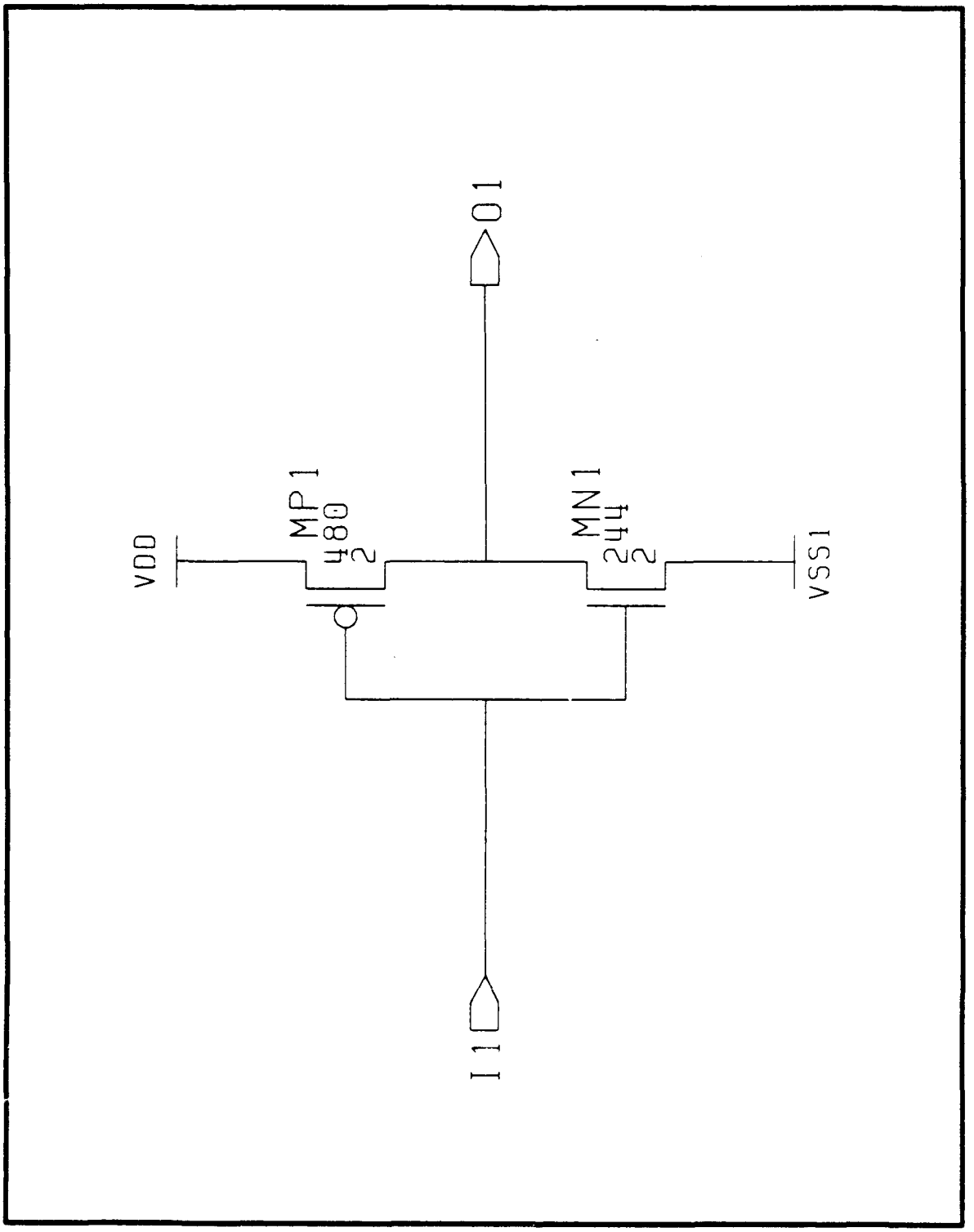


Figure 98 RLOS Test Vehicle (B,C) Primitive Inverter

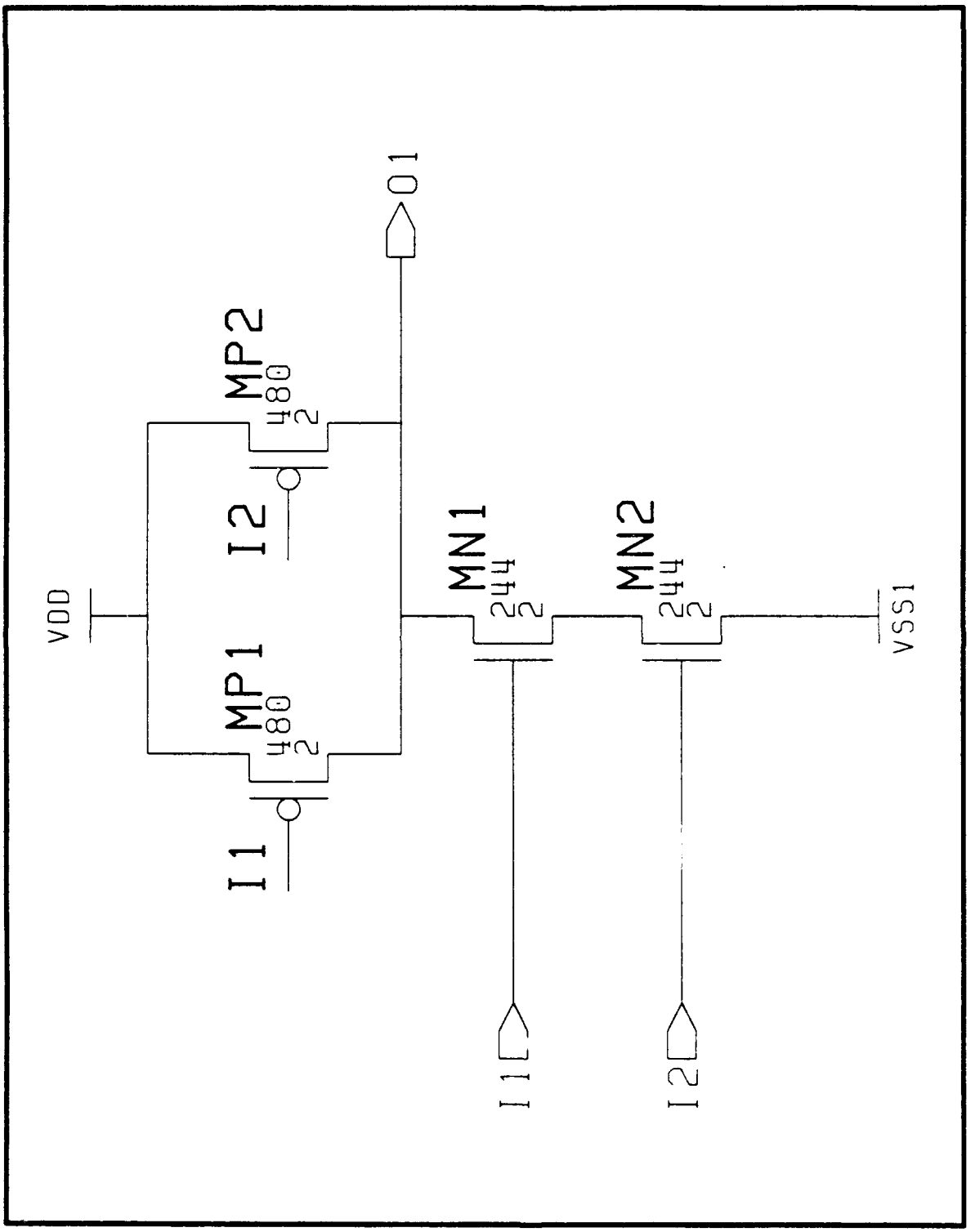


Figure 99 RLOS Test Vehicle (B,C) Primitive 2-Input NAND

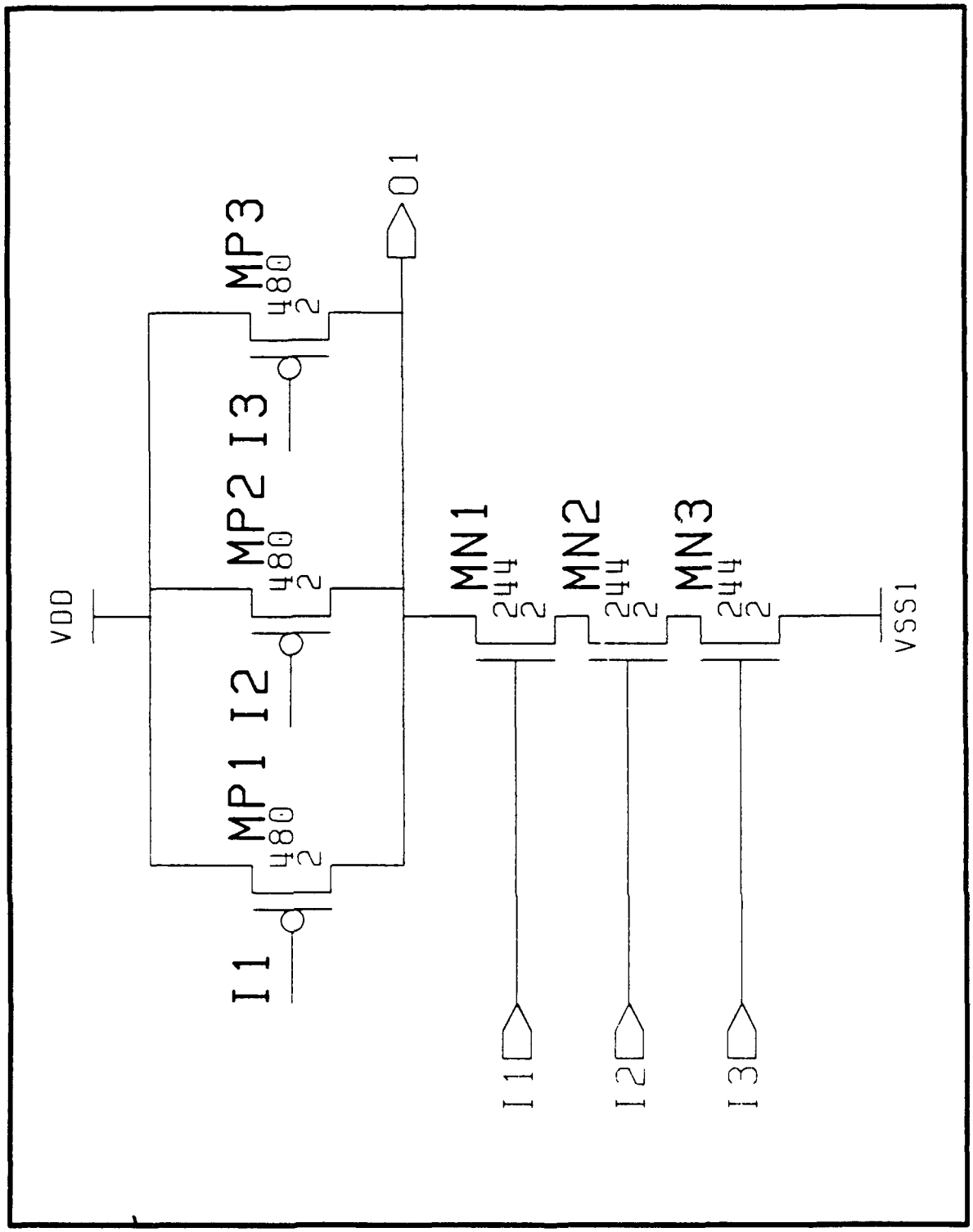


Figure 100 RLOS Test Vehicle (B,C) Primitive 3-Input NAND

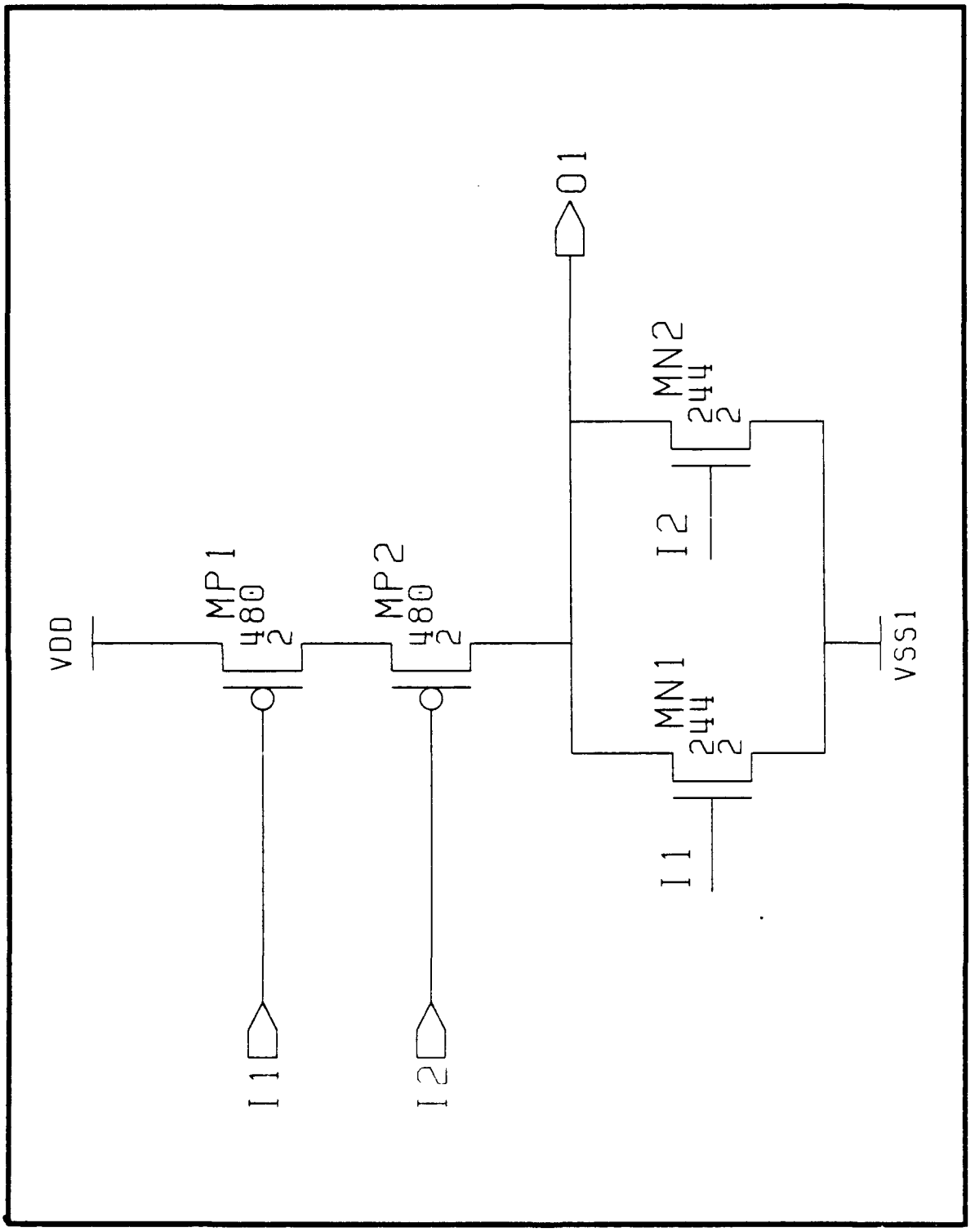


Figure 101 RLOS Test Vehicle (B,C) Primitive 2-Input NOR

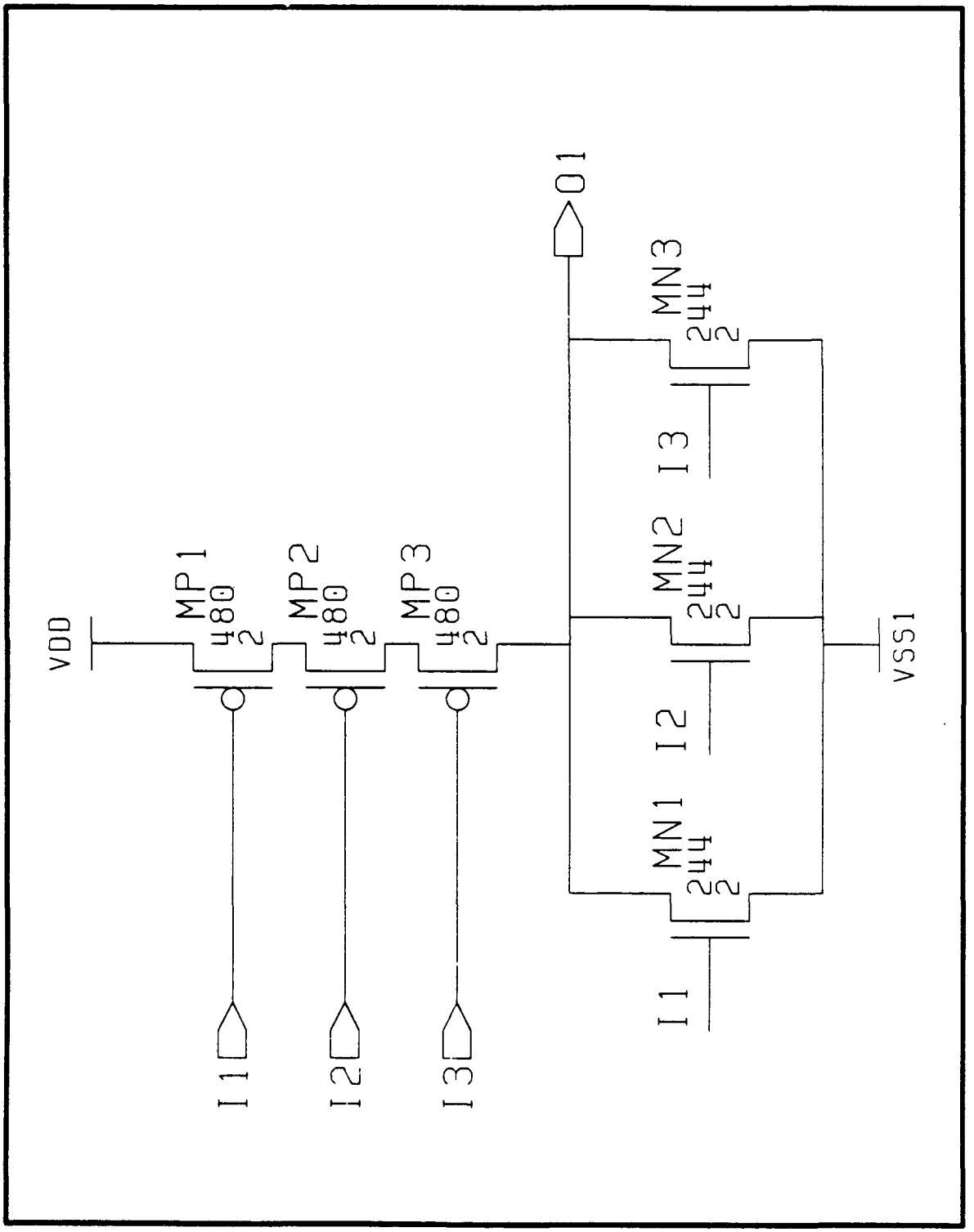


Figure 102 RLOS Test Vehicle (B,C) Primitive 3-Input NOR

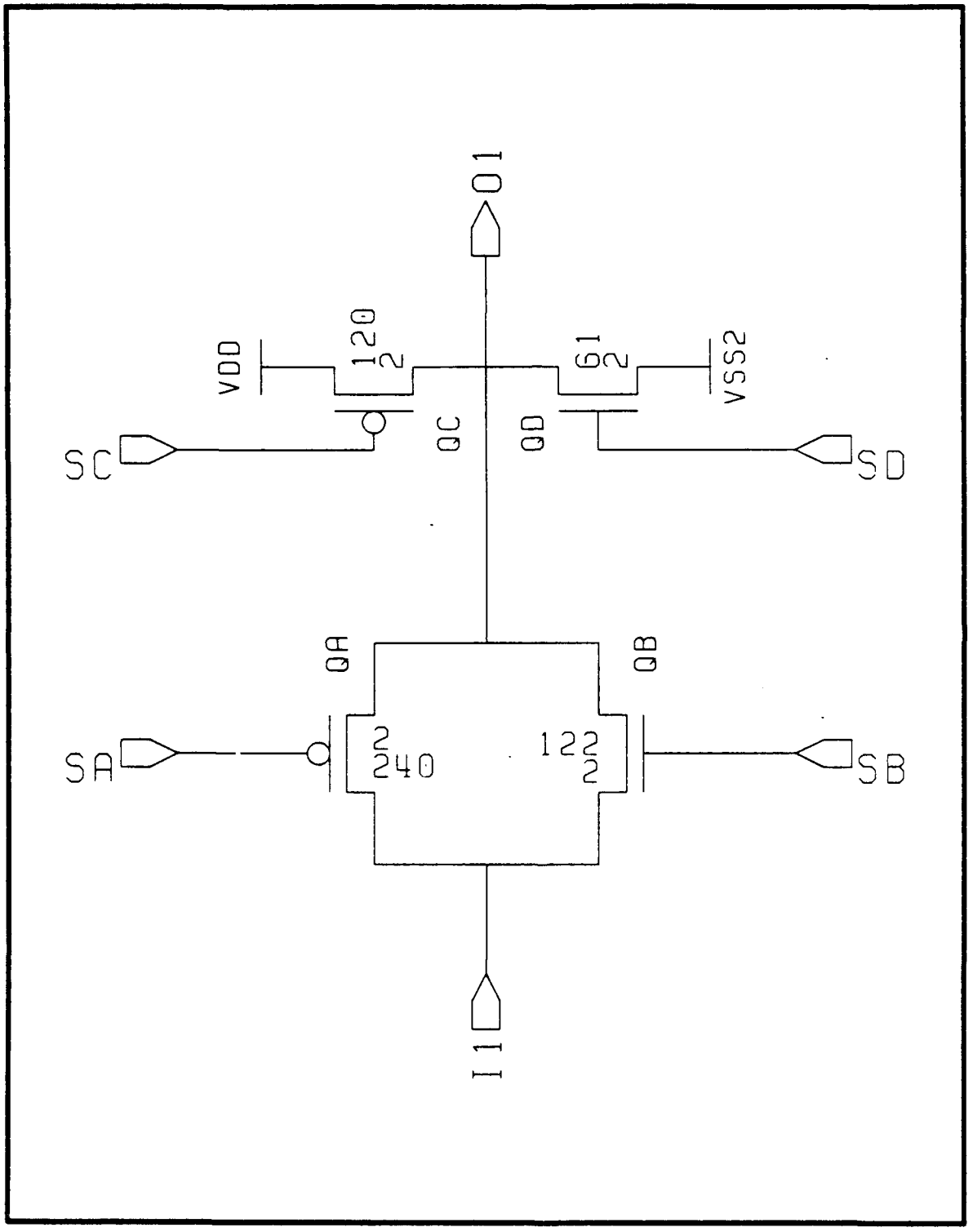


Figure 103 RLOS Test Vehicle B Stress Control Circuit

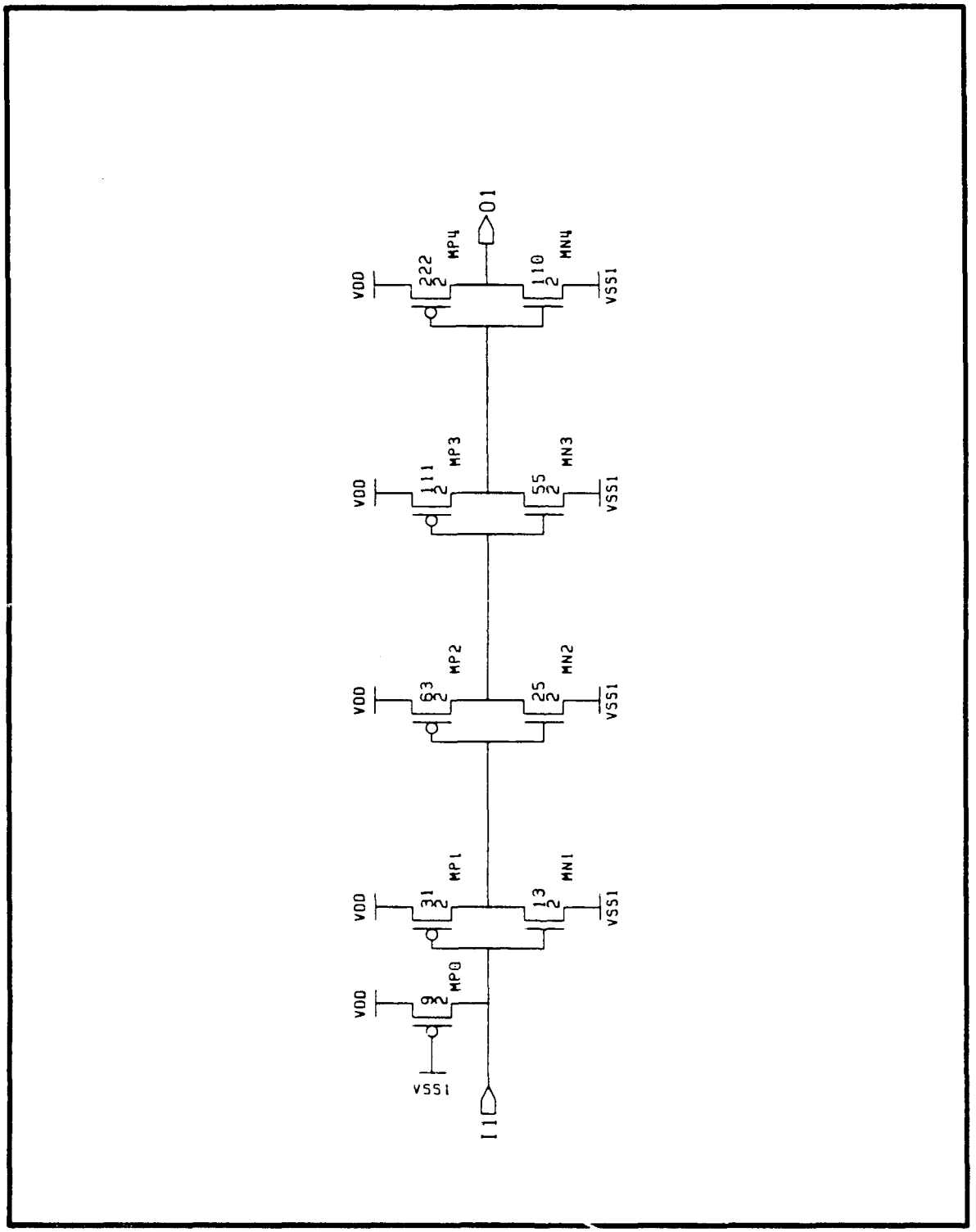


Figure 104 RLOS Test Vehicle (B,C) Input Pad

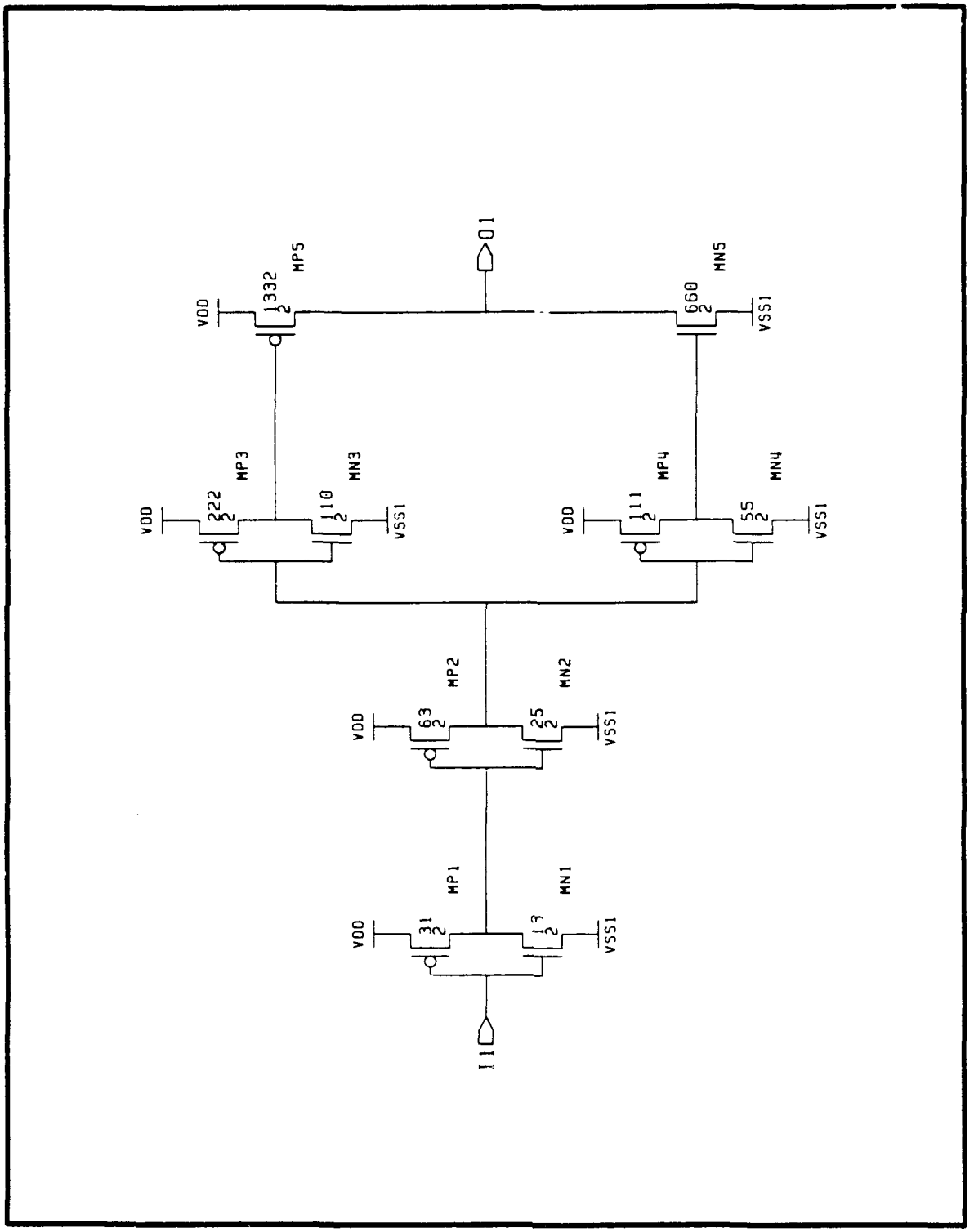


Figure 105 RLOS Test Vehicle (B,C) Output Pad

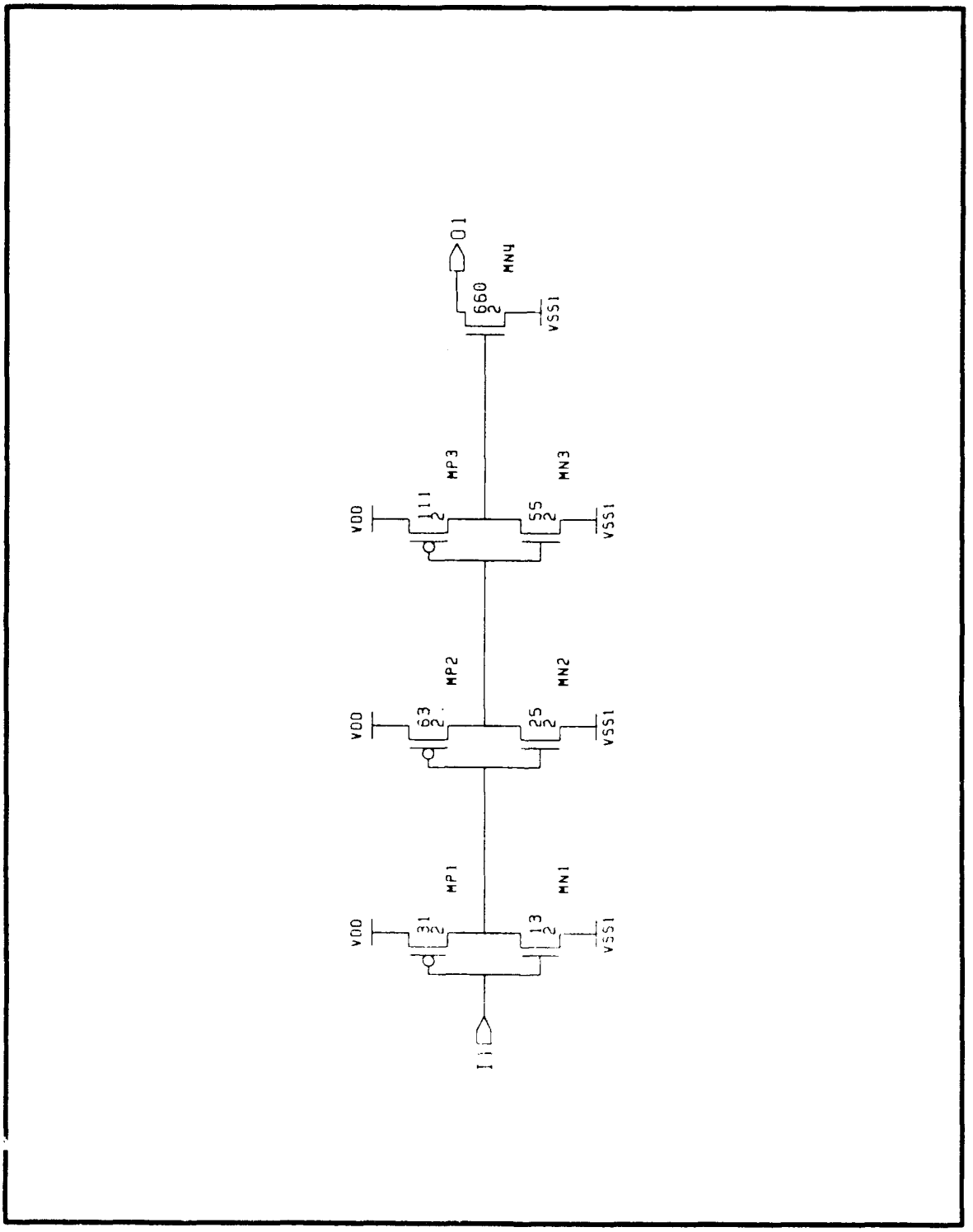


Figure 106 RLOS Test Vehicle (B,C) Open Drain Output Pad

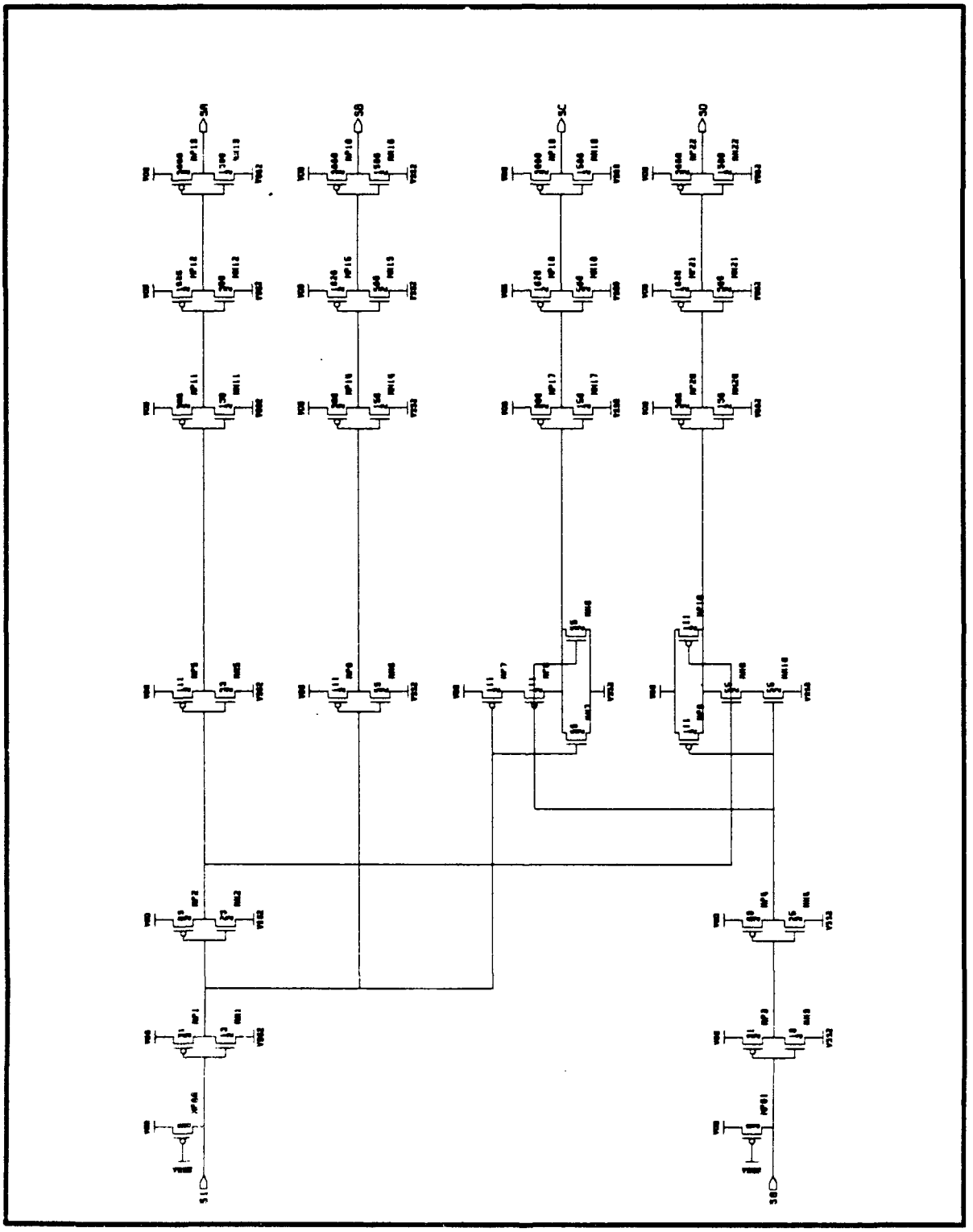


Figure 107 RLOS Test Vehicle B Stress Input Pad

D. Life/Screen Test Detailed Schematics

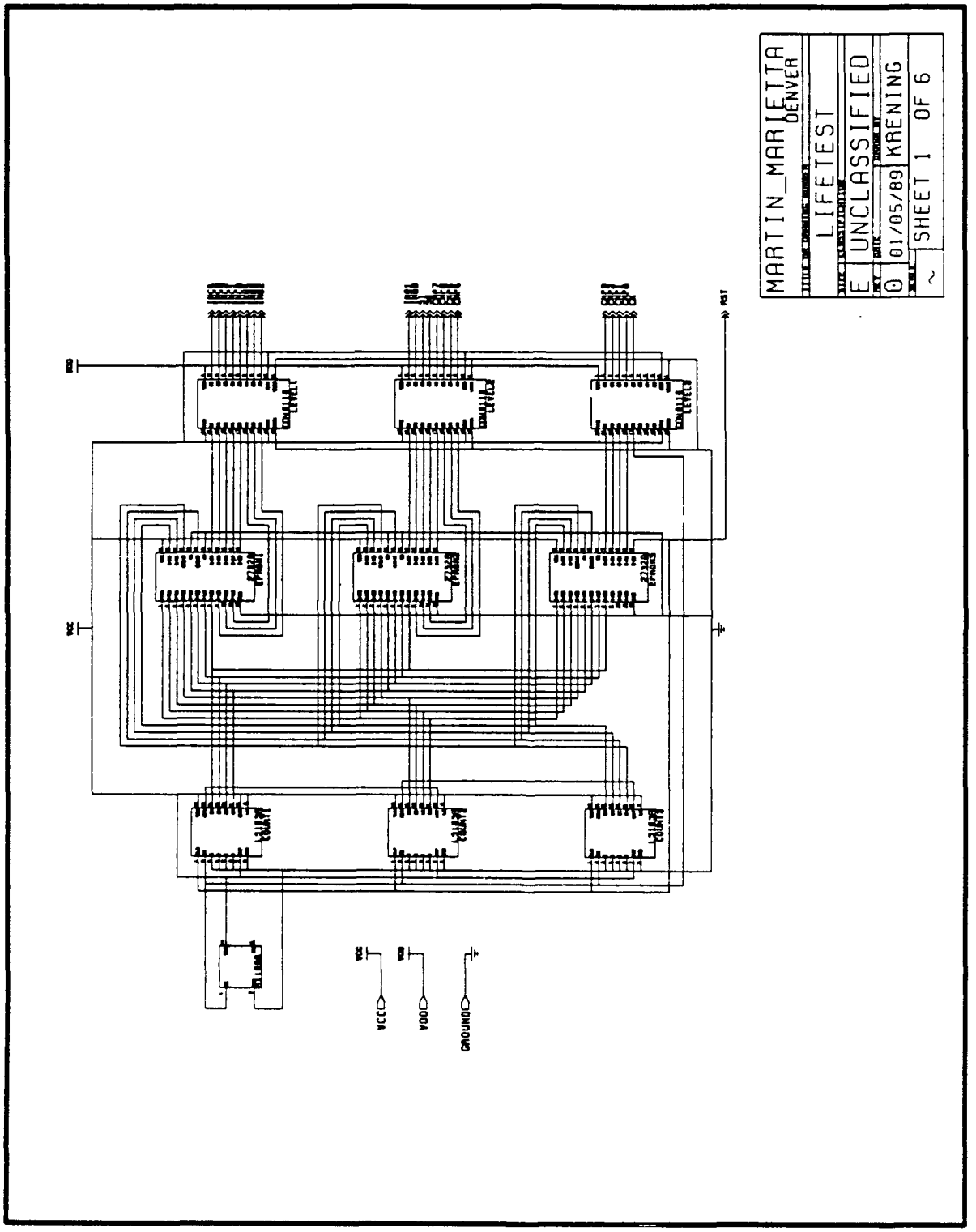


Figure 108 RLOS Lifetest Board Sheet 1

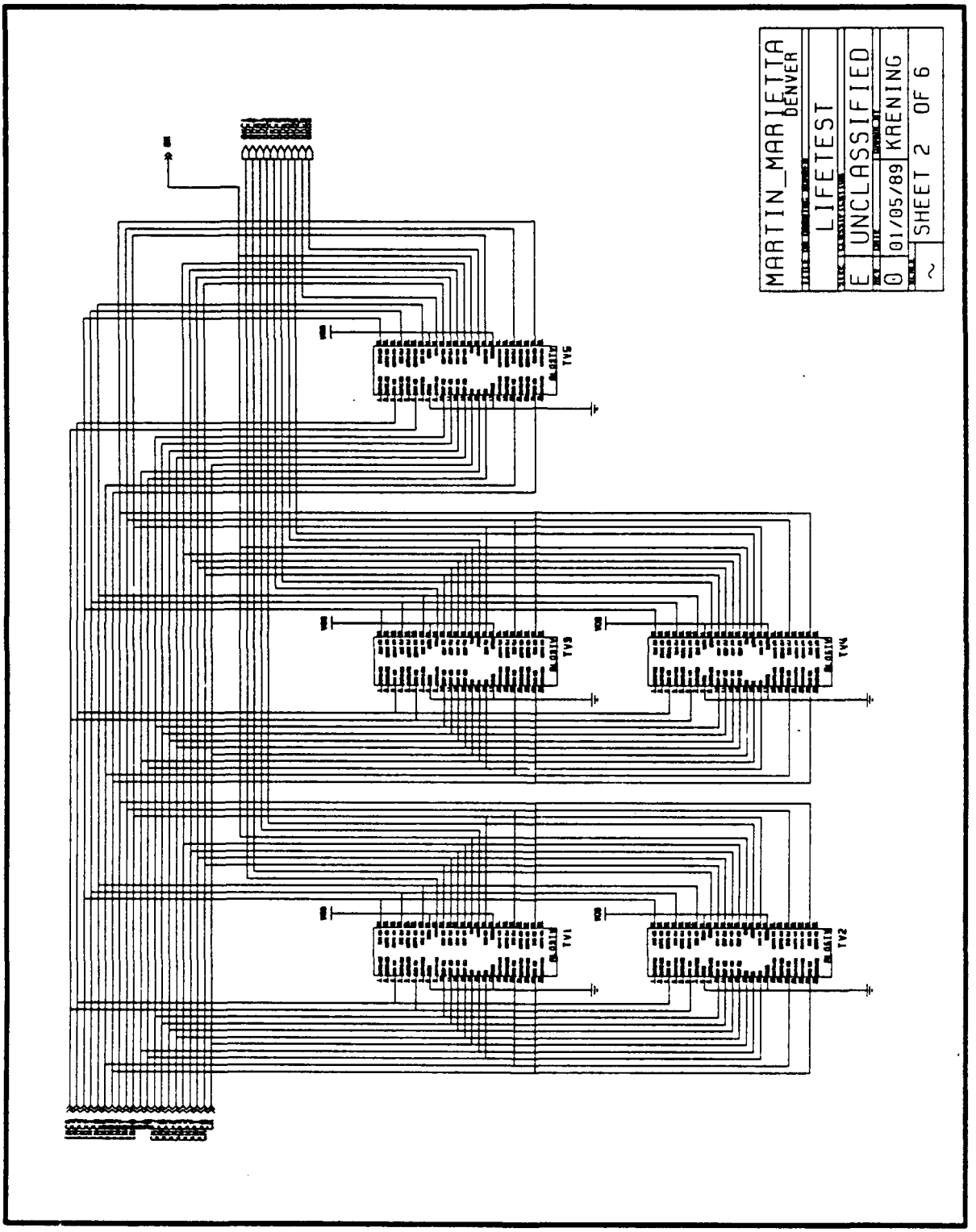


Figure 109 RLOS Lifetest Board Sheet 2

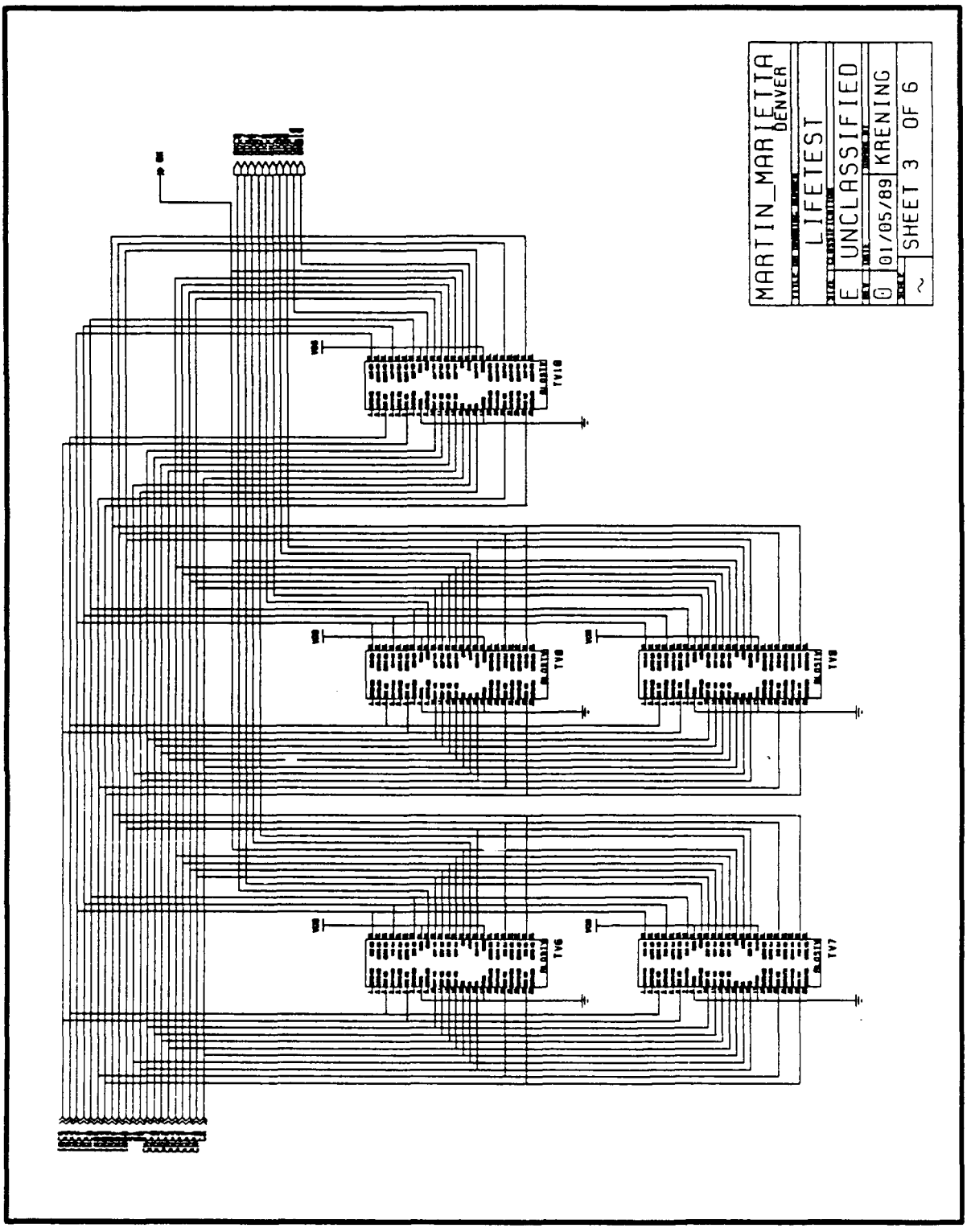


Figure 110 RLOS Lifetest Board Sheet 3

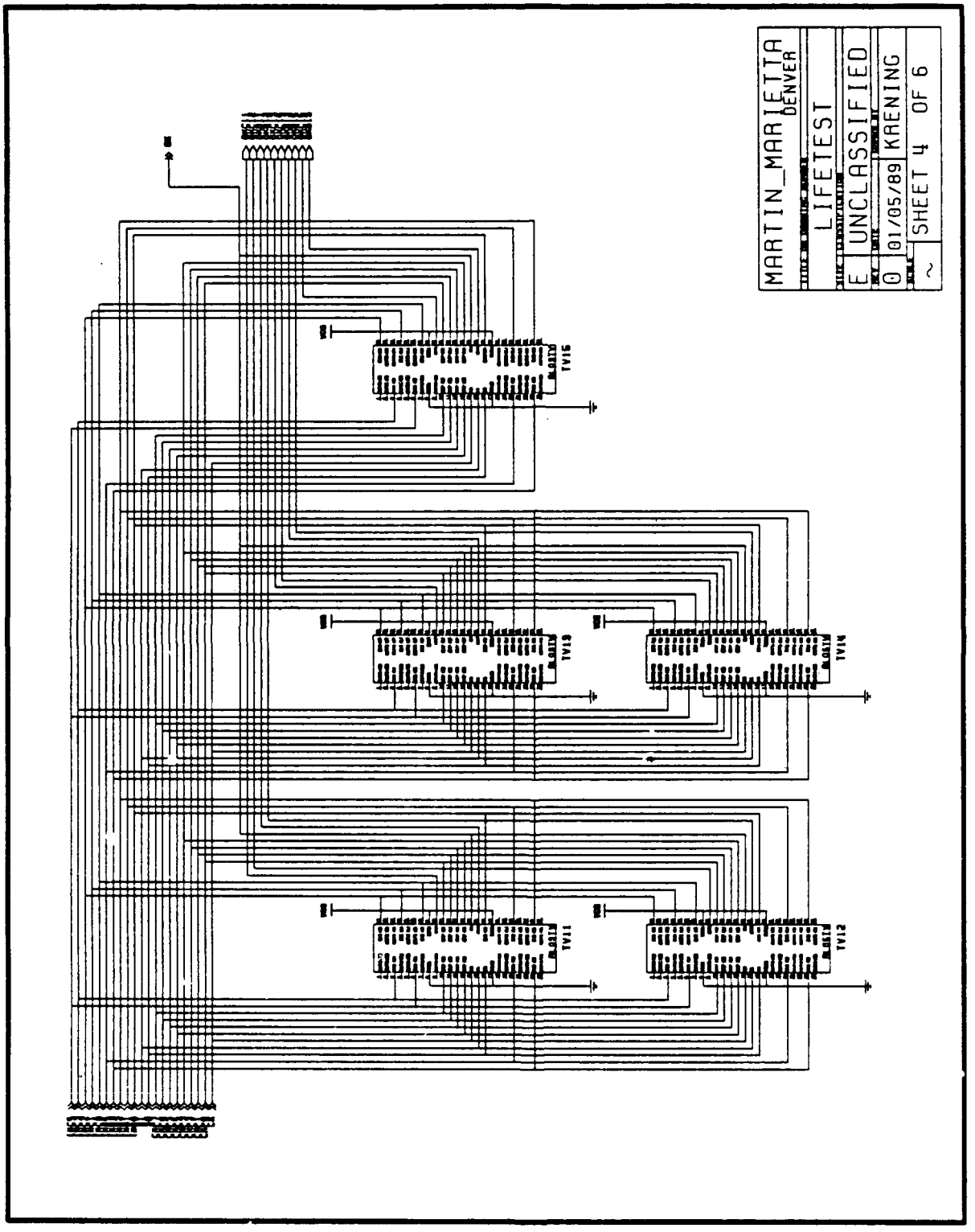


Figure 111 RLOS Lifetest Board Sheet 4

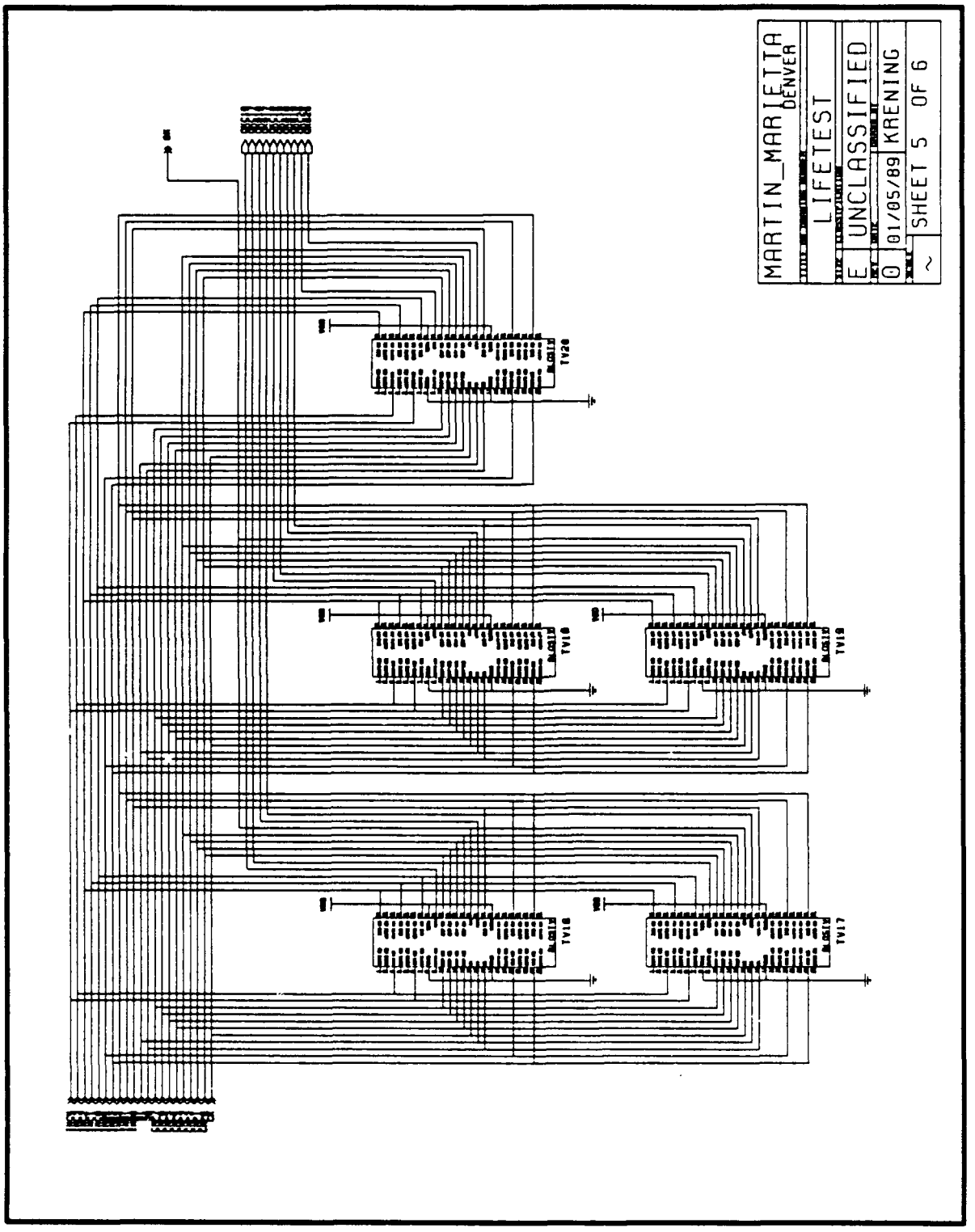


Figure 112 RLOS Lifetest Board Sheet 5

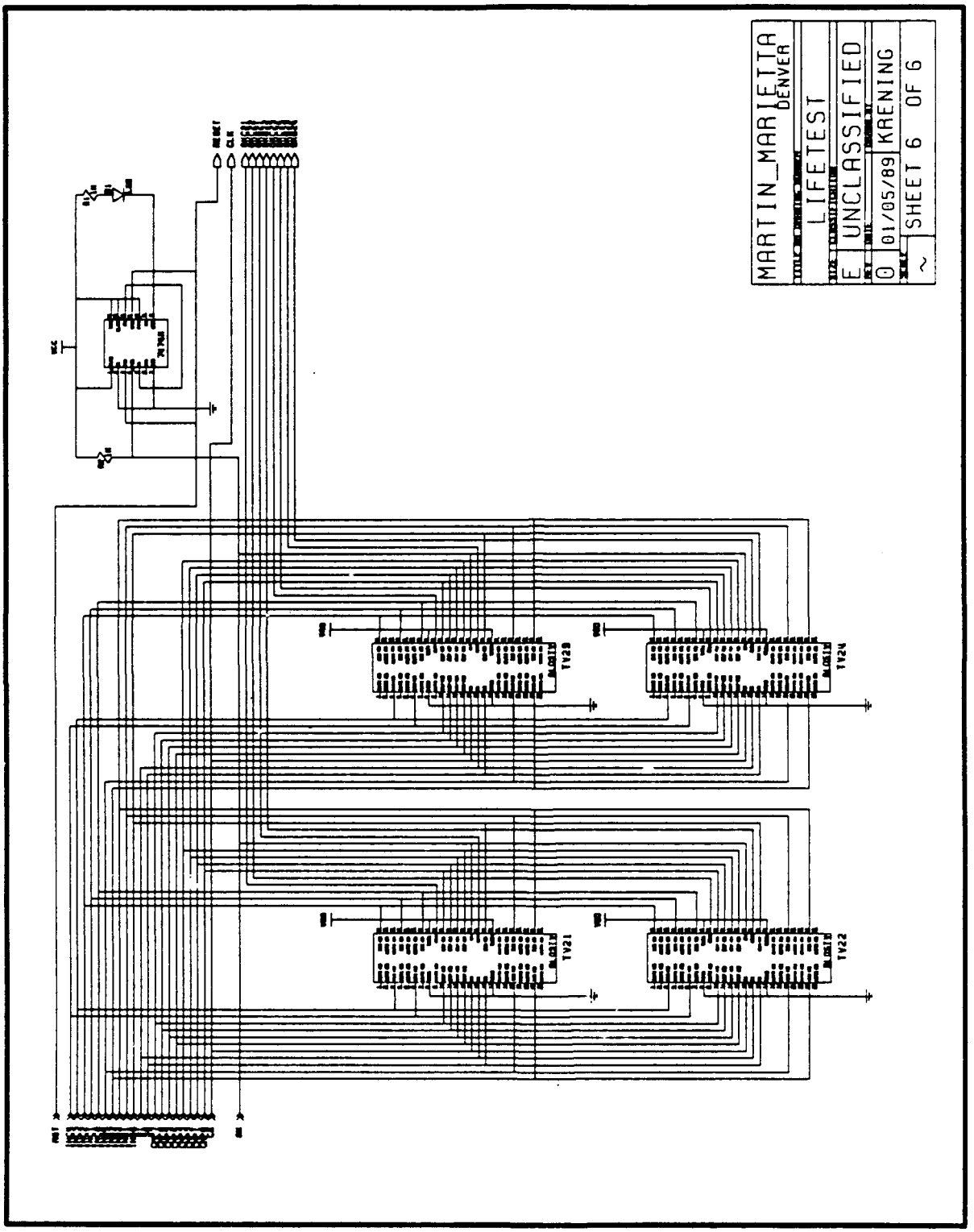


Figure 113 RLOS Lifetest Board Sheet 6

E. RLOSTV Test Pattern Set

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0000.0400 432104321076543210    CCCCCCCCCCBBBBBBBBBB
0000.0500                       9876543210987654321O
0000.0600
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0179.0000 1001110011000100110101LLLLHLLLHHLLLLHLLLHHHHH
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0183.0000 10001100010101001100 0LHLLHLLLHHLHLLHLLLHHHHH
0184.0000 10001100011010110000 1LHLLHLLLHHLHLLHLLLHHHHH
0185.0000 10001100011010110000 0LHLLHLLLHHLHLLHLLLHHLLL
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0197.0000 00000000000111010011 0HLLLLHLLHHLLLLLLLLLLLLL
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0199.0000 00001000010101001101 0LHLLHLLLHHLHLLHLLLHHHHH
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0201.0000 00001000011010110010 0LHLLHLLLHHHHHHHHHHHHLHL
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0207.0000 00011000110001001110 0LLLLHLLLHHHHHHHHHHHHHHH
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0342.0000 10101101010101001101OLHLLHLLLHHLHLLHLLLHHHHH
0343.0000 10101101010101001101OLHLLHLLLHHLHLLHLLLHHHHH
0344.0000 10101101011010110010OLHLLHLLLHHHHHHHHHHHHLHL
0345.0000 10101101011010110010OLHLLHLLLHHHHHHHHHHHHLHL
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0347.0000 10101101010101001111OLHLLHLLLHHLLLLLLLLLLHLL
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0383.0000 1000010000100010111110HLLLLHLLHHLLLLLLLLLLHLL
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F. Initial Electrical Characterization Plots

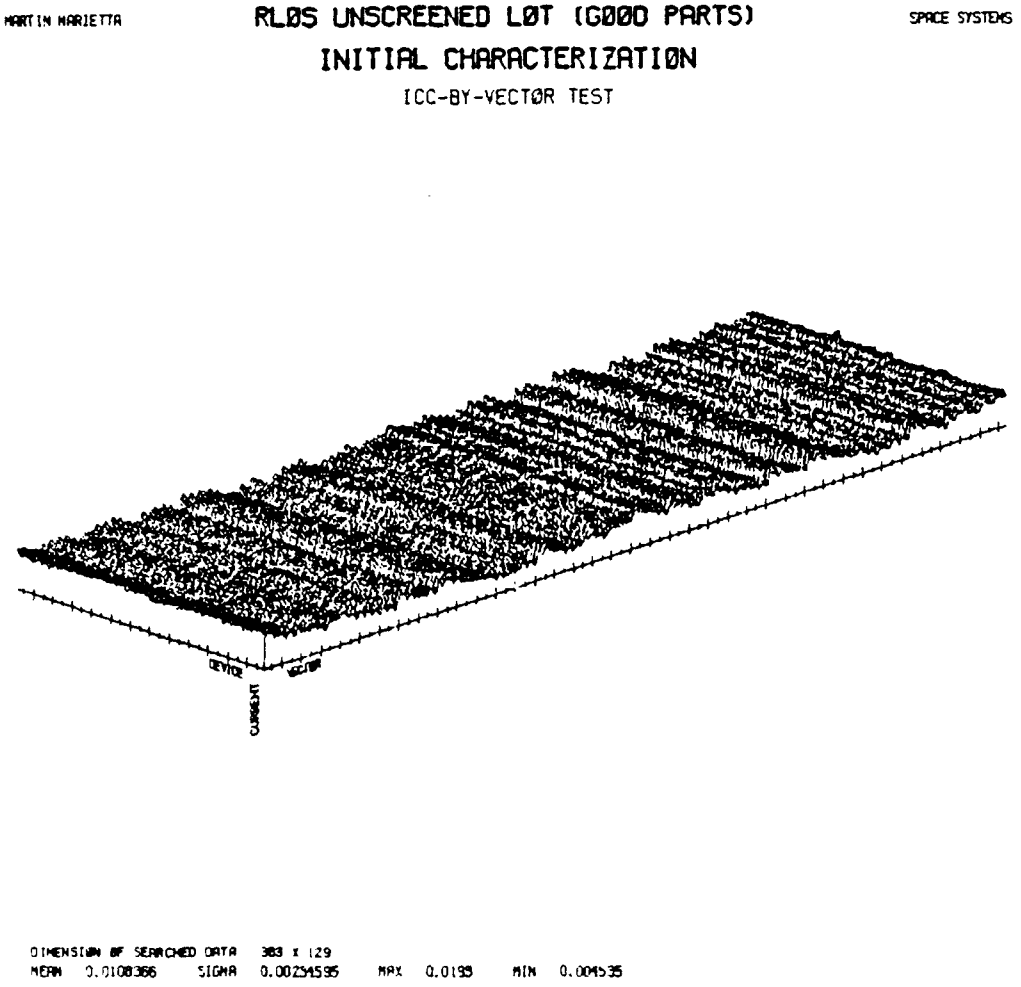

Figure 114 Overview of ICC vs Test Vector, Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

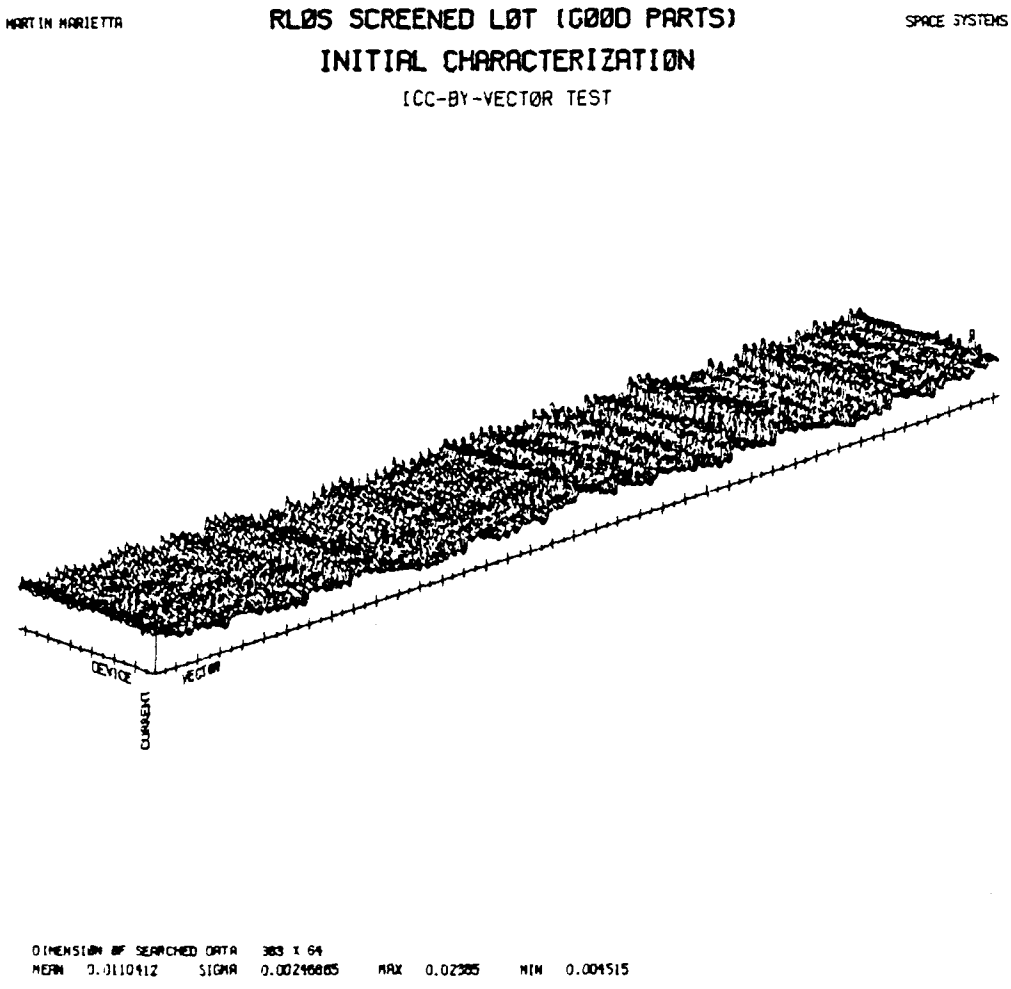

Figure 115 Overview of ICC vs Test Vector, Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

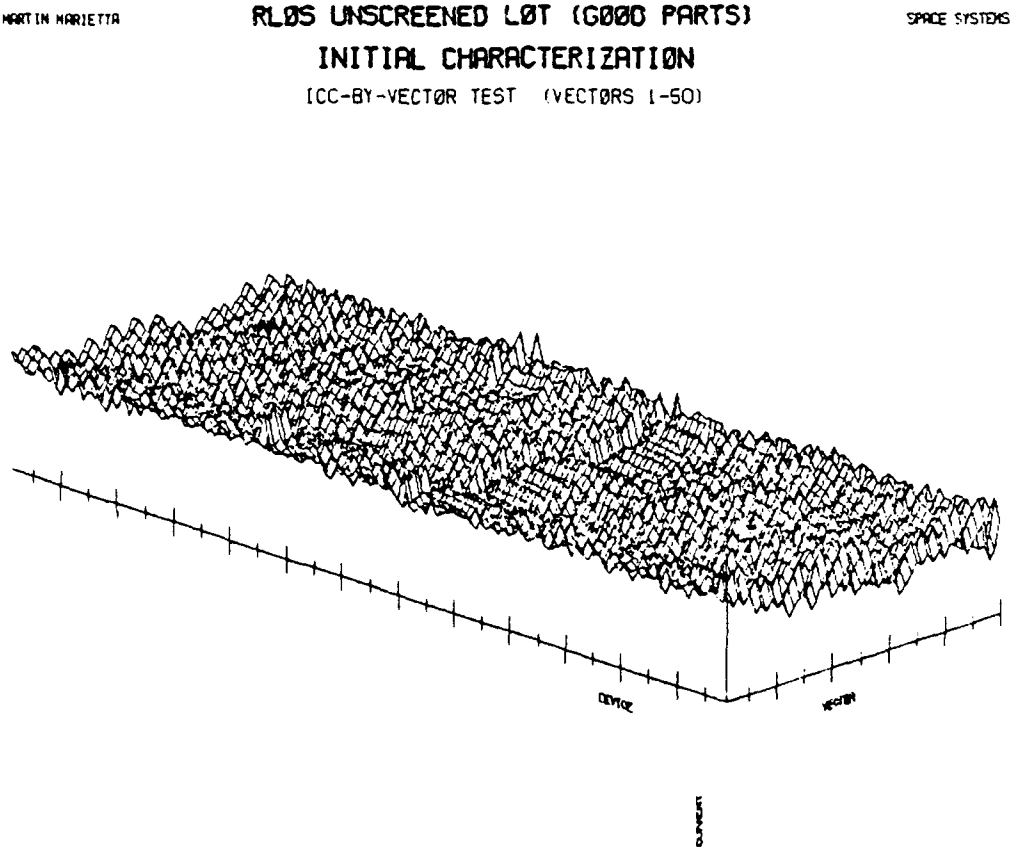

Figure 116 ICC vs Test Vector (1-50), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

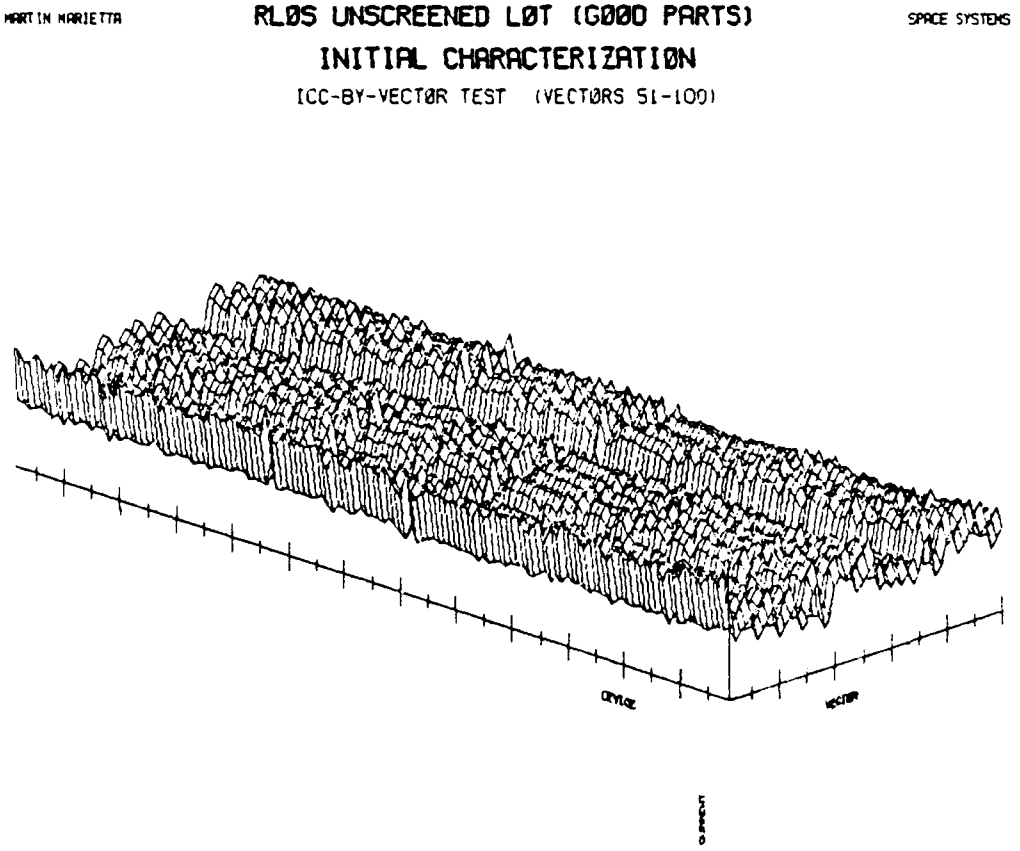

Figure 117 ICC vs Test Vector (51-100), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

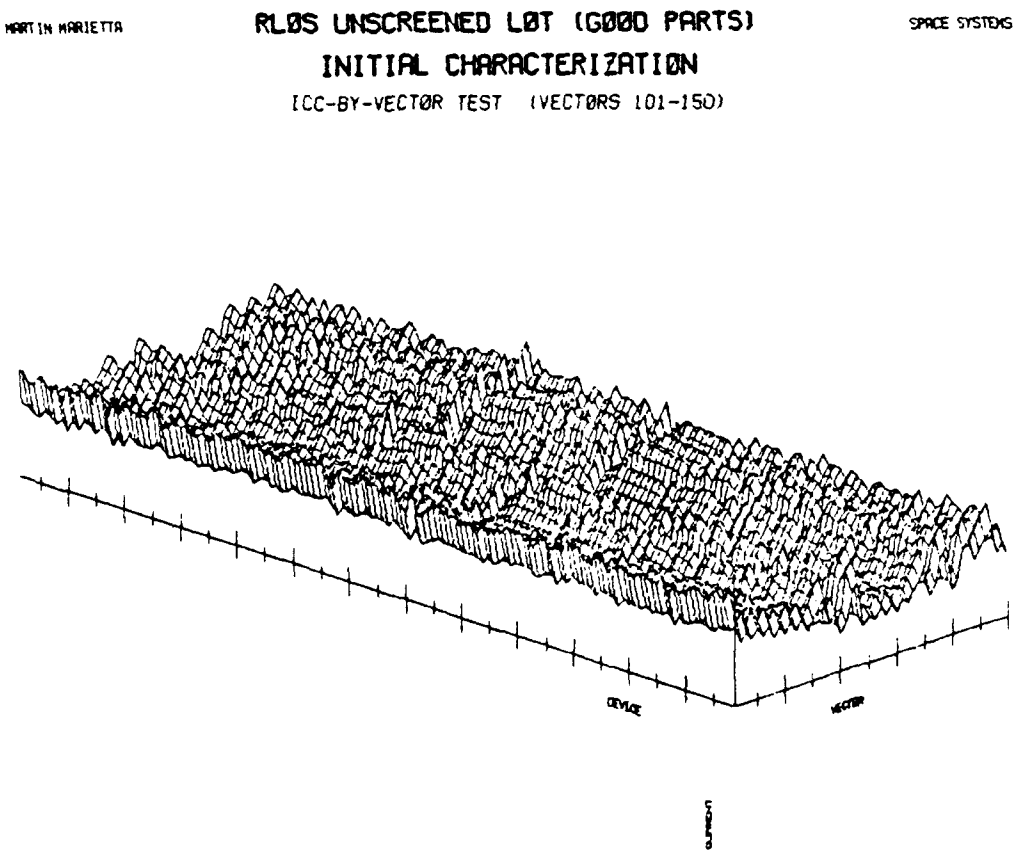

Figure 118 ICC vs Test Vector (101-150), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

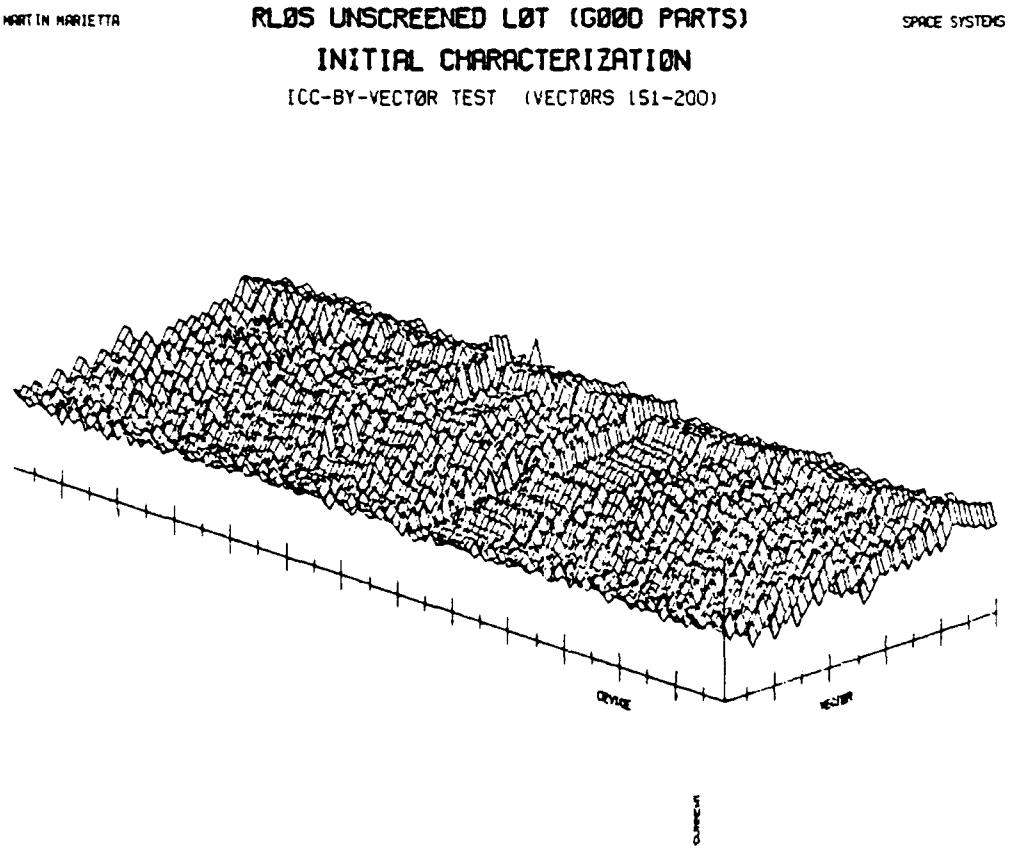

Figure 119 ICC vs Test Vector (151-200), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

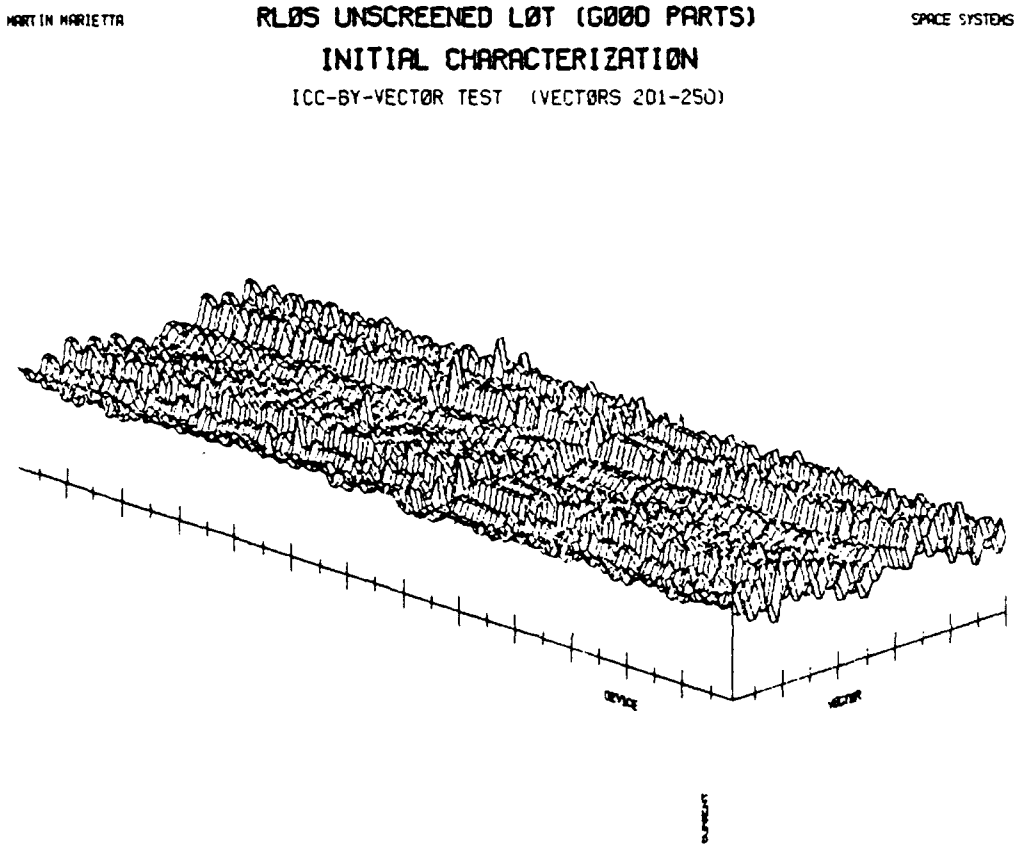

Figure 120 ICC vs Test Vector (201-250), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

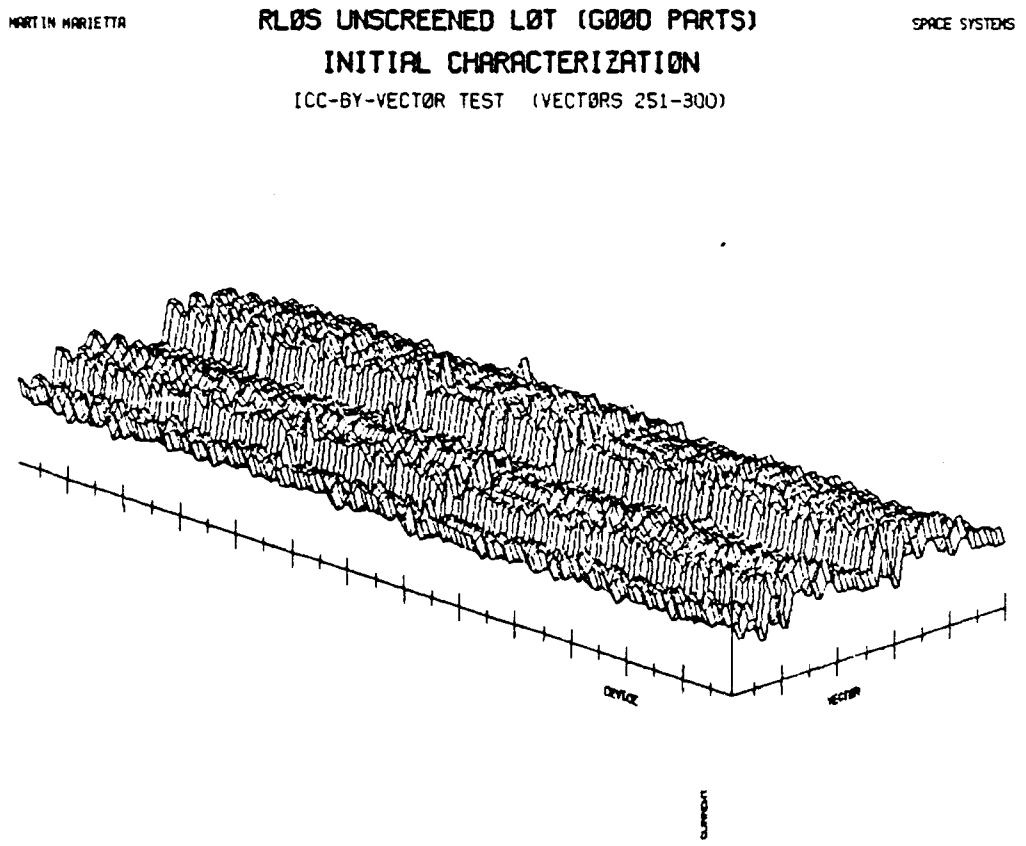

Figure 121 ICC vs Test Vector (251-300), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

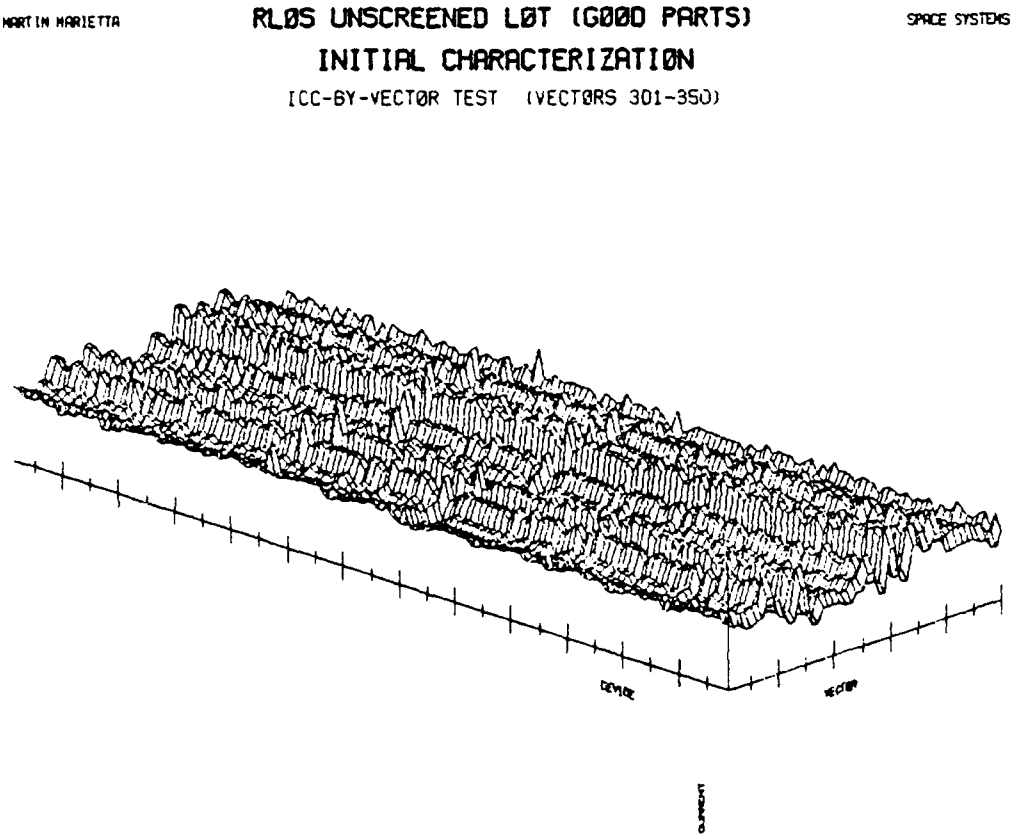

Figure 122 ICC vs Test Vector (301-350), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

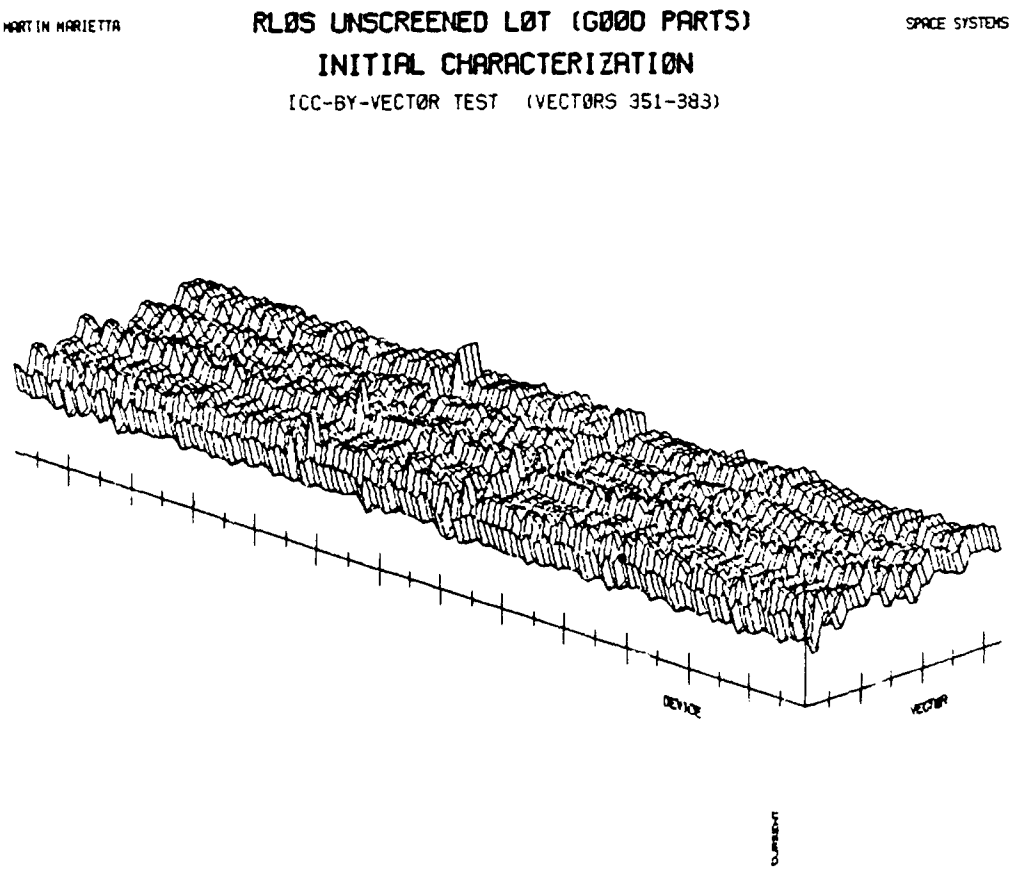

Figure 123 ICC vs Test Vector (351-383), Unscreened Lot, Initial Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-129
Z-Axis: ICC 0-20 mA

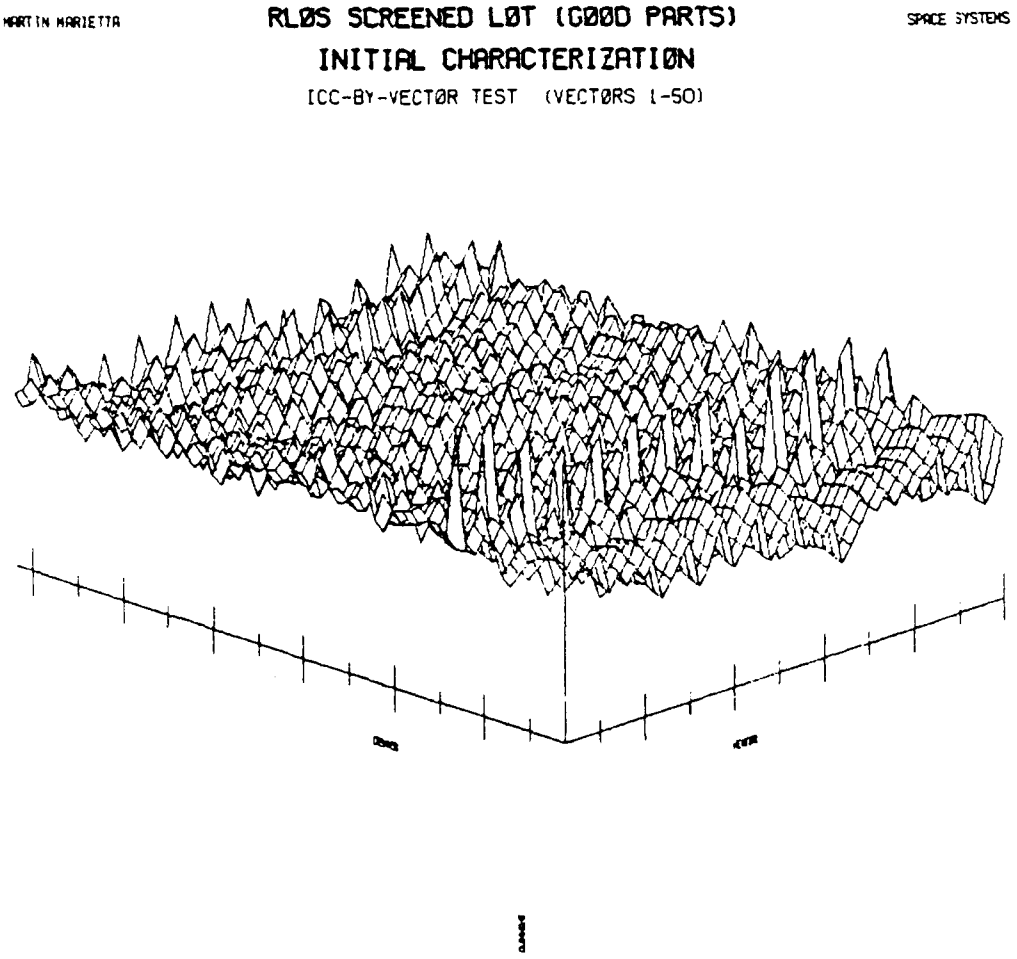

Figure 124 ICC vs Test Vector (1-50), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

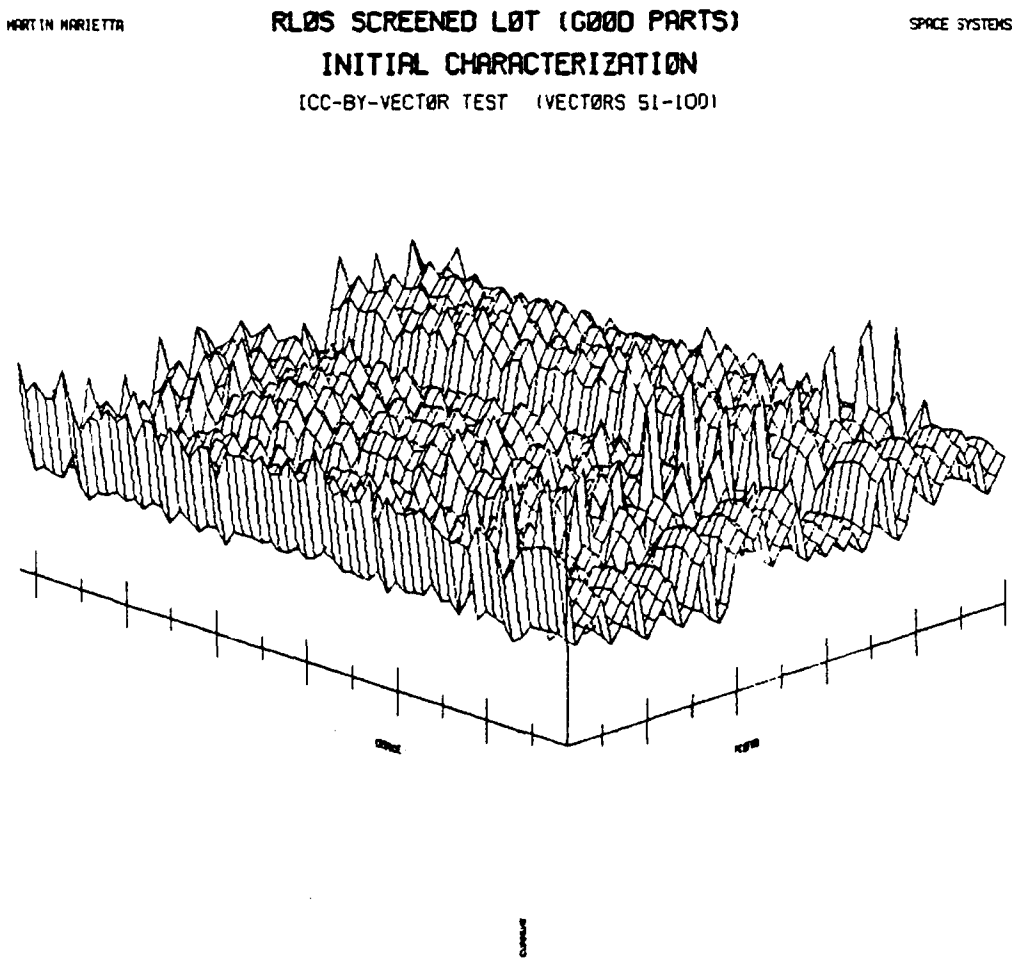

Figure 125 ICC vs Test Vector (51-100), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

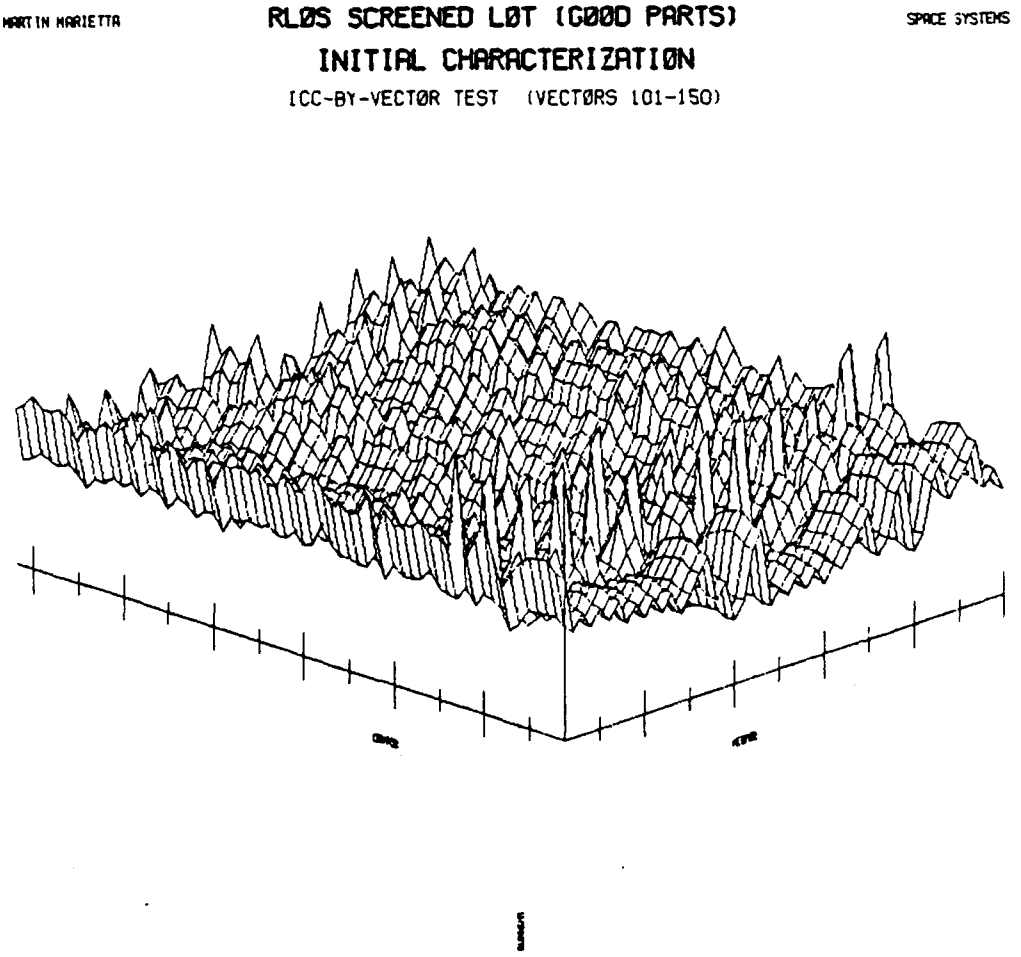

Figure 126 ICC vs Test Vector (101-150), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

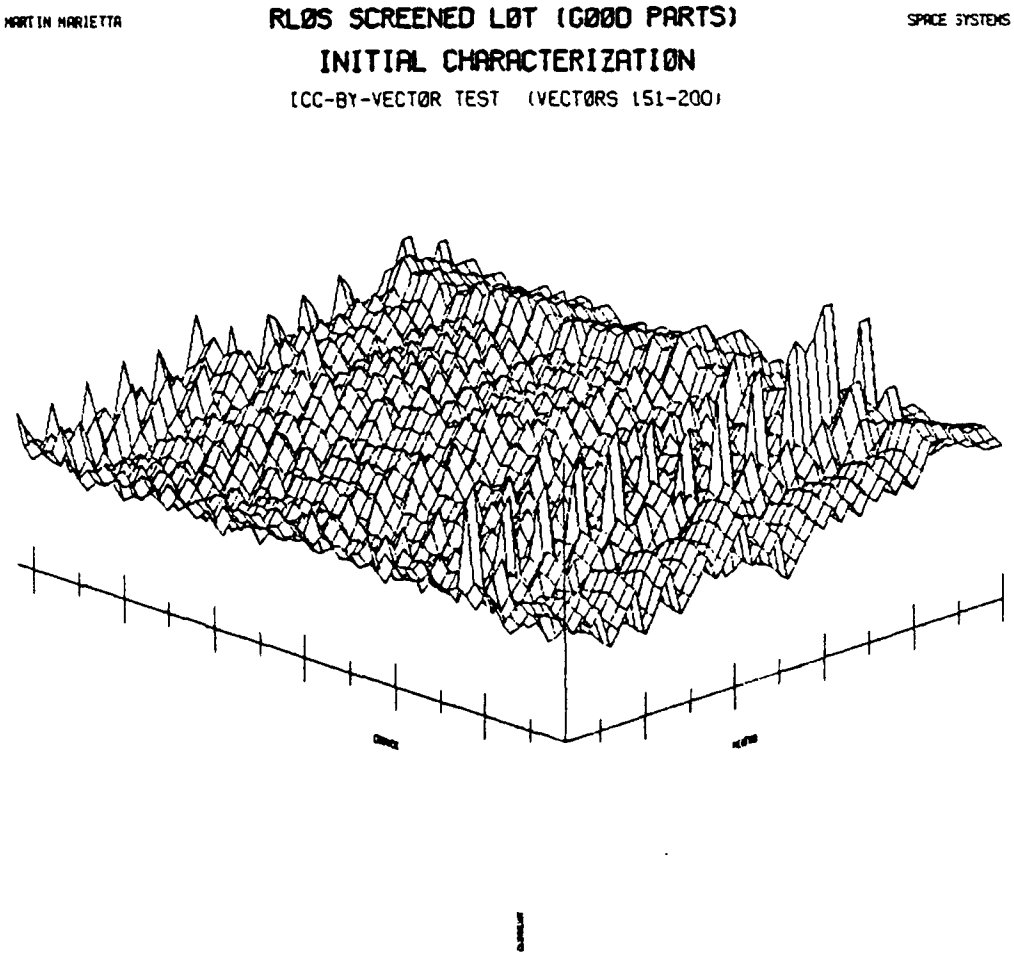

Figure 127 ICC vs Test Vector (151-200), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

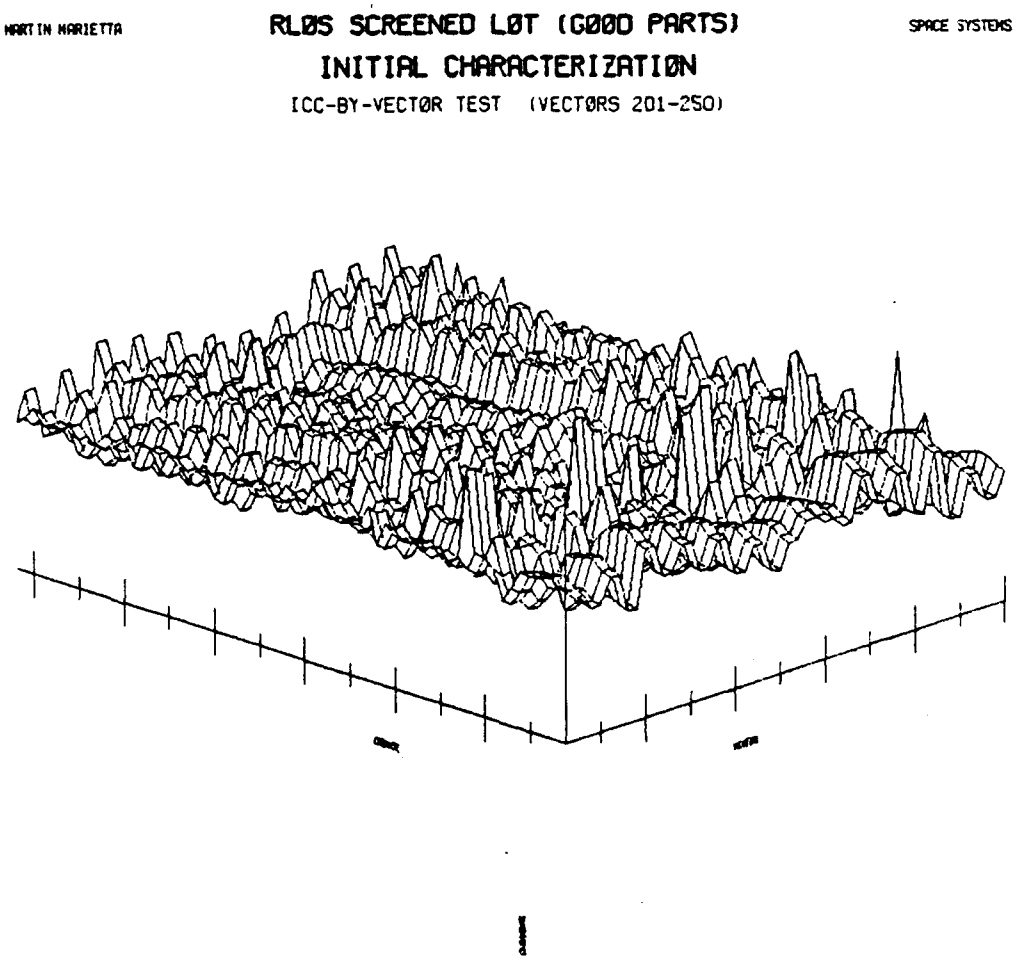

Figure 128 ICC vs Test Vector (201-250), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

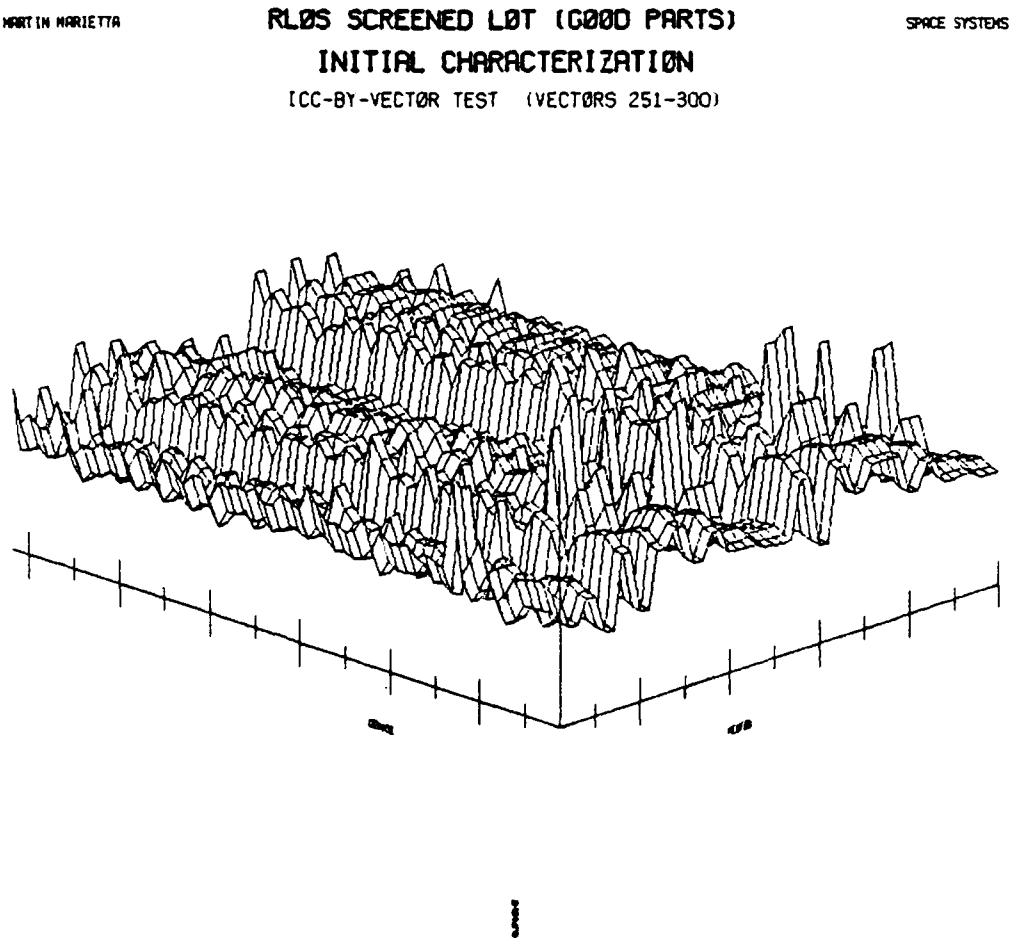

Figure 129 ICC vs Test Vector (251-300), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

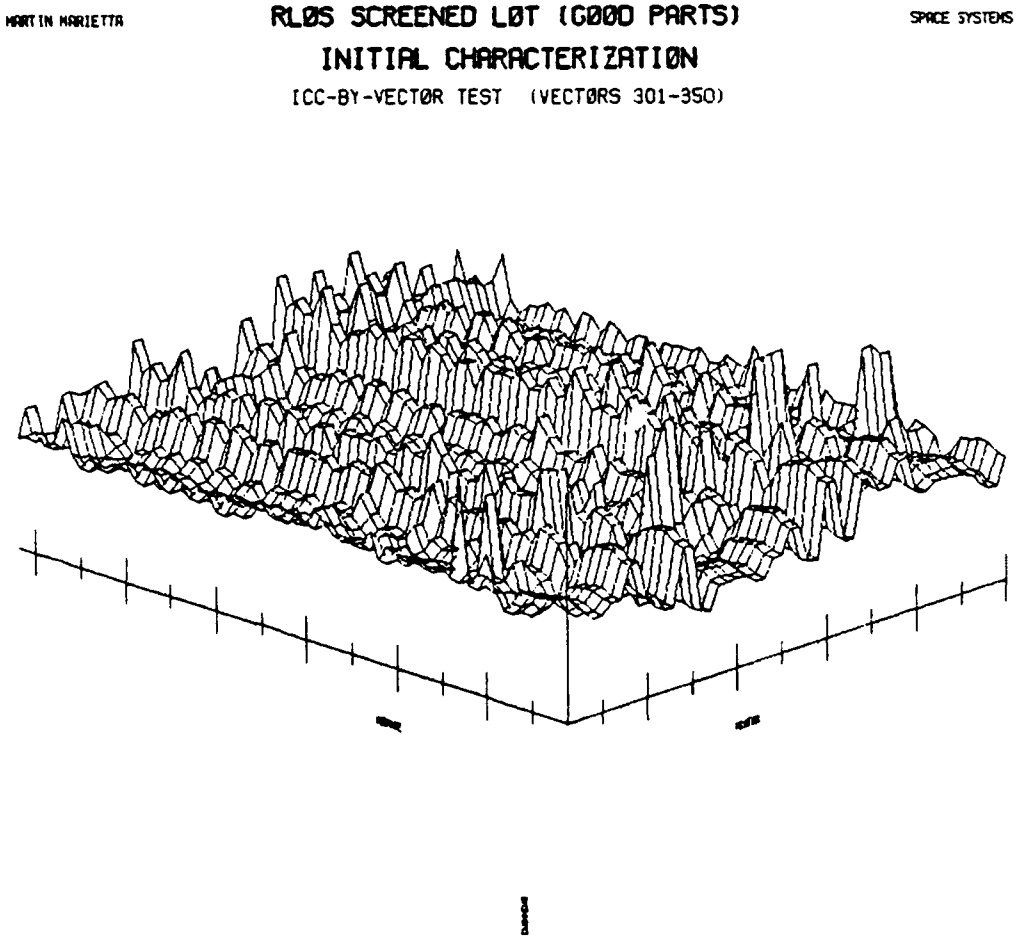

Figure 130 ICC vs Test Vector (301-350), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

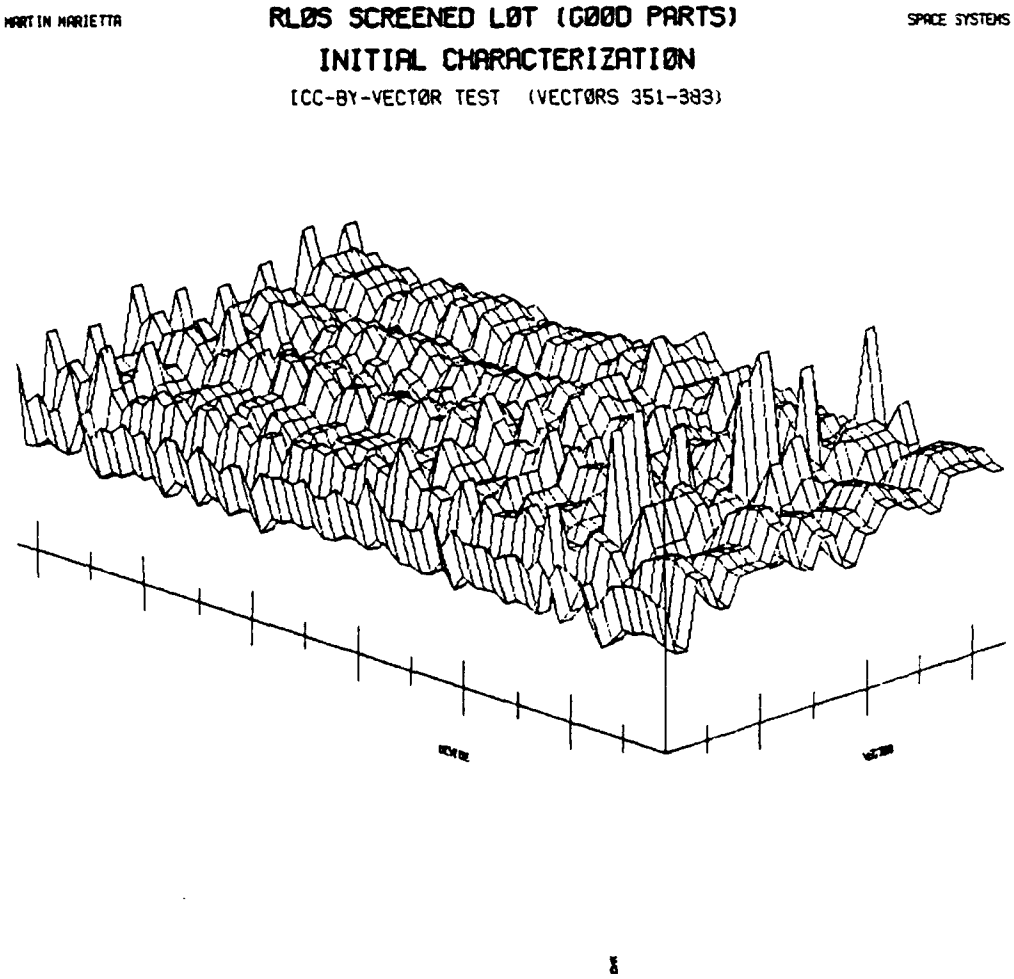

Figure 131 ICC vs Test Vector (351-383), Screened Lot, Initial Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-63
Z-Axis: ICC 0-25 mA

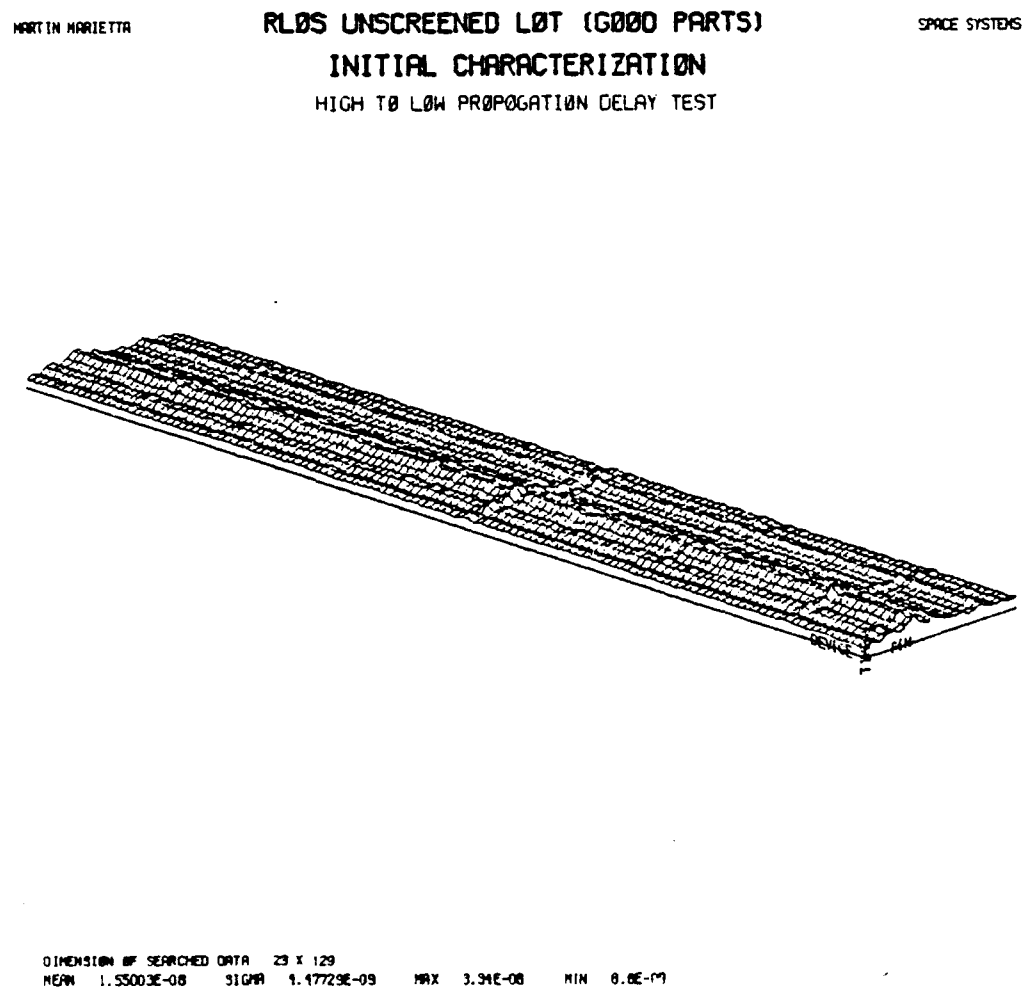

Figure 132 High to Low Propagation Delays, Unscreened Lot, Initial Data

Plot Information:

X-Axis: Pins 1-23
Y-Axis: Devices 1-129
Z-Axis: Tphl 0-35 nS

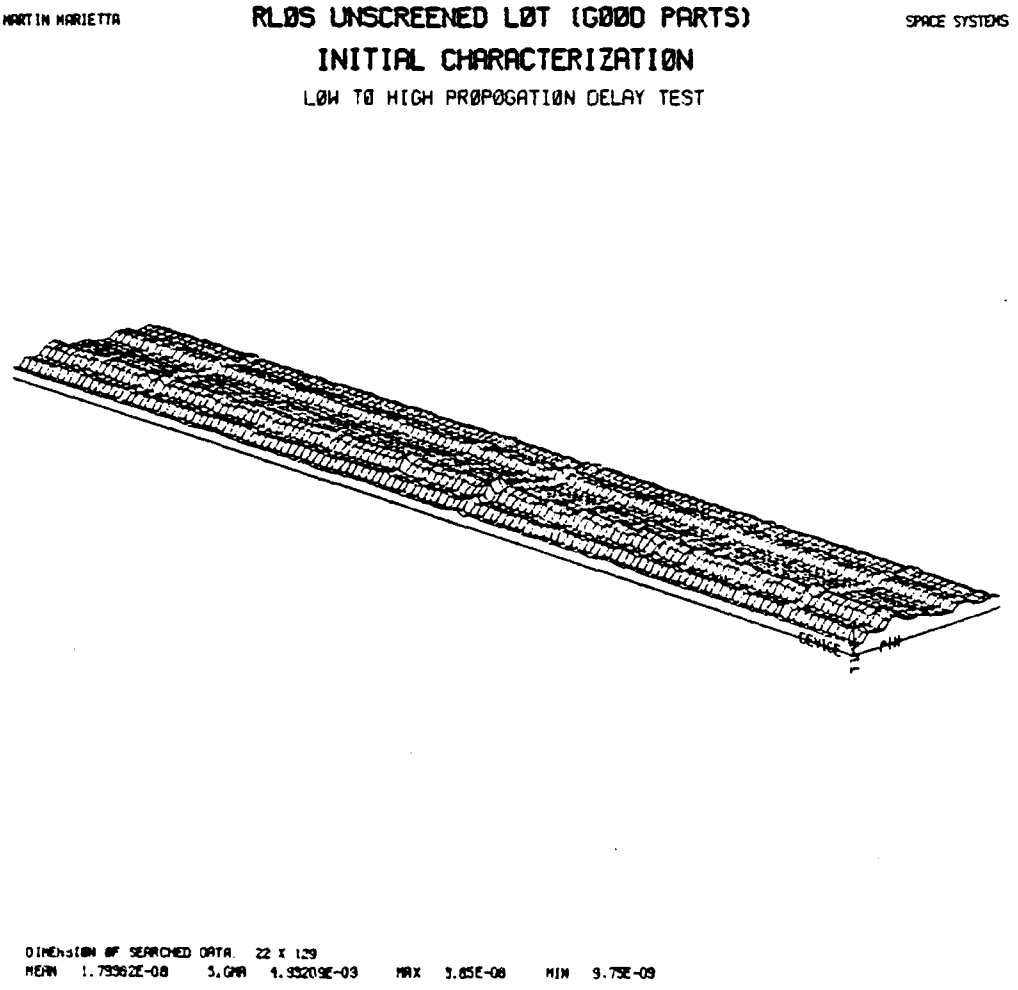

Figure 133 Low to High Propagation Delays, Unscreened Lot, Initial Data

Plot Information:

X-Axis: Pins 1-22
Y-Axis: Devices 1-129
Z-Axis: Tplh 0-40 nS

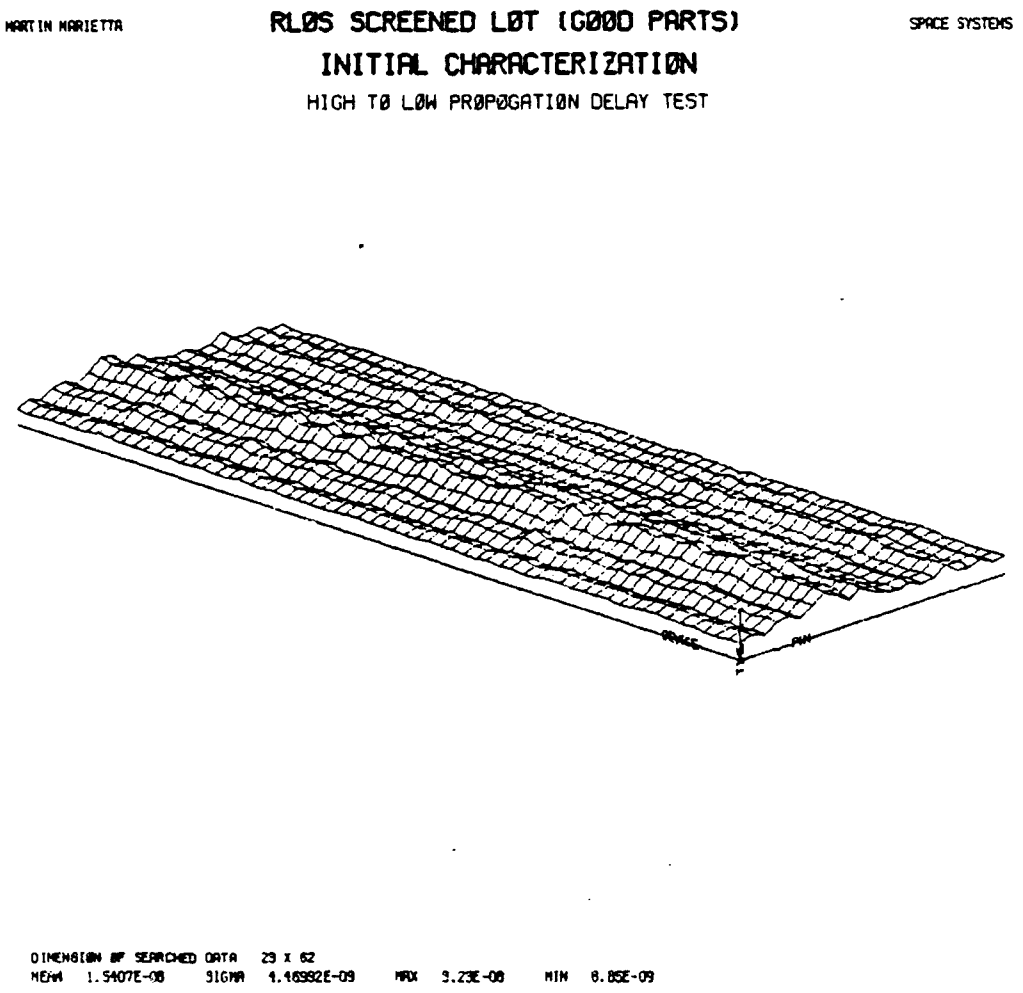

Figure 134 High to Low Propagation Delays, Screened Lot, Initial Data

Plot Information:

X-Axis: Pins 1-23
Y-Axis: Devices 1-63
Z-Axis: Tphl 0-35 nS

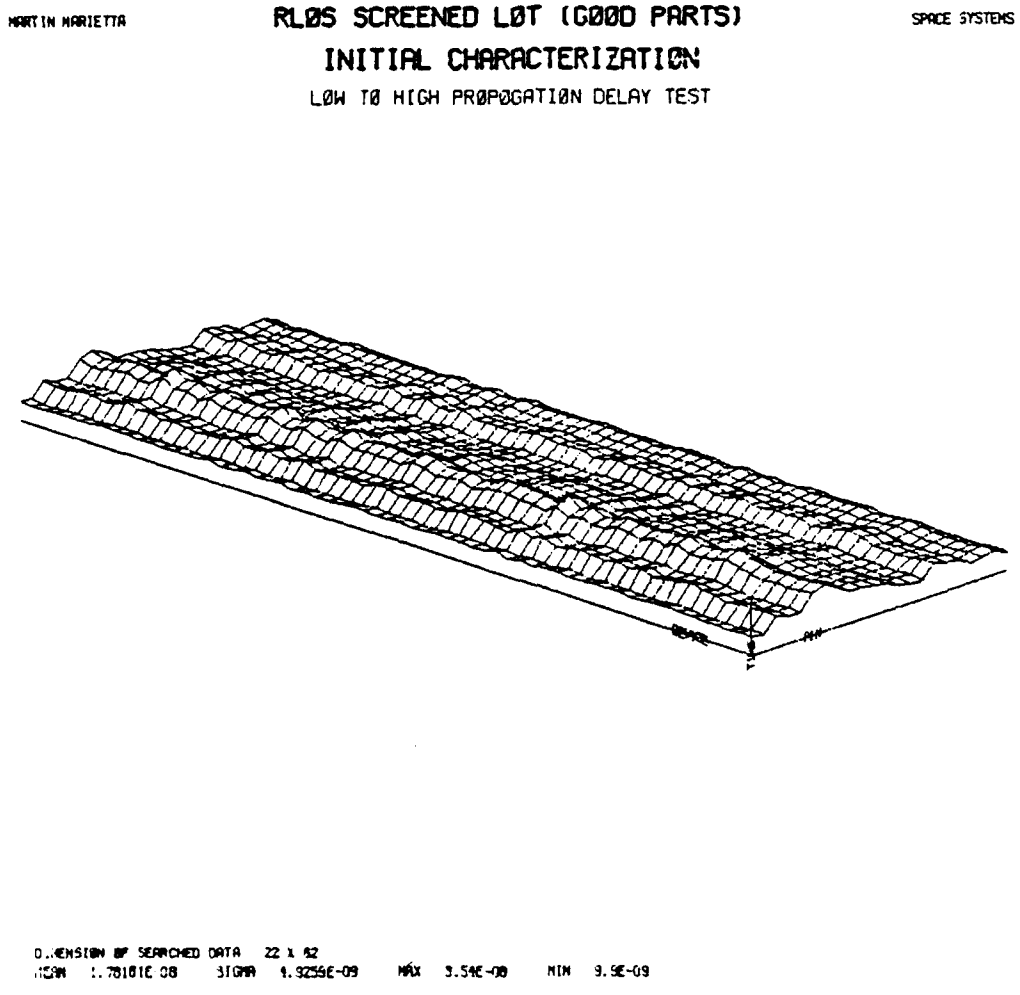

Figure 135 Low to High Propagation Delays, Screened Lot, Initial Data

Plot Information:

X-Axis: Pins 1-22
Y-Axis: Devices 1-63
Z-Axis: Tplh 0-35 nS

G. Final Electrical Characterization Plots

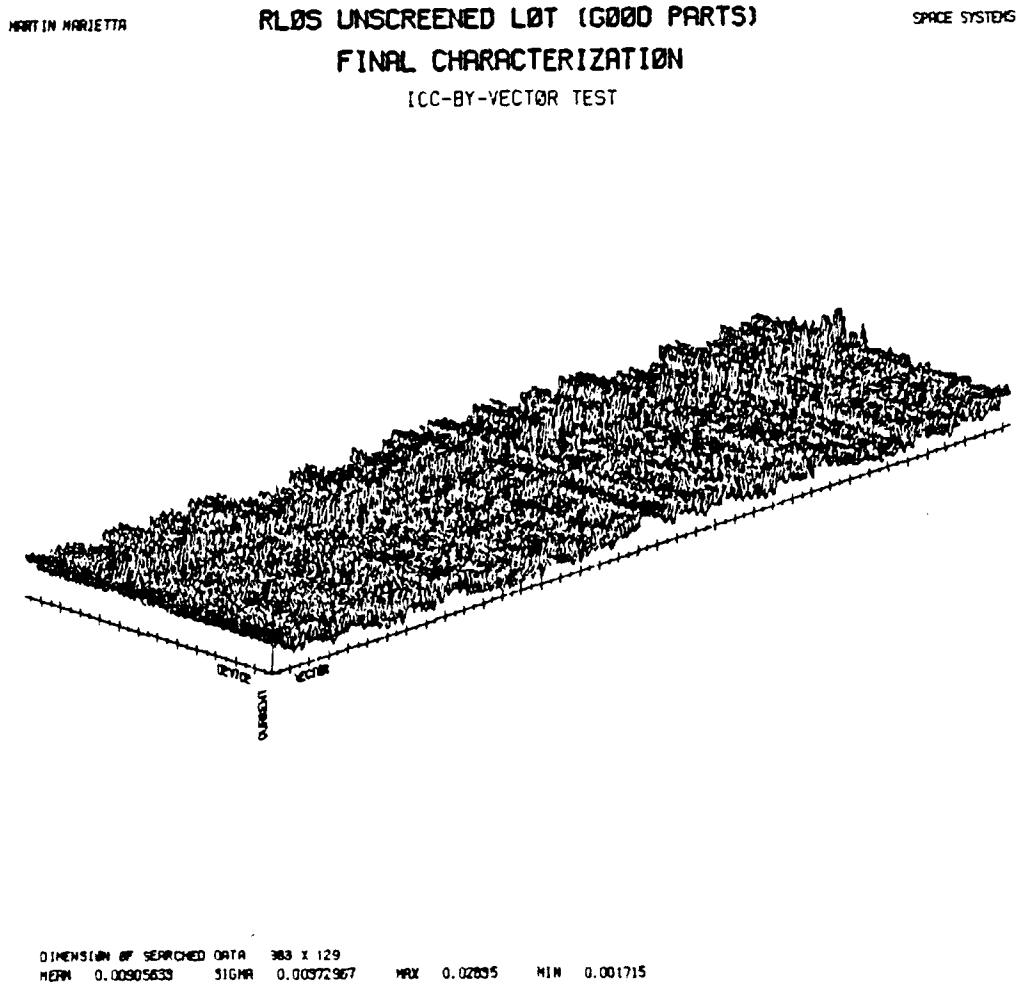

Figure 136 Overview of ICC vs Test Vector, Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

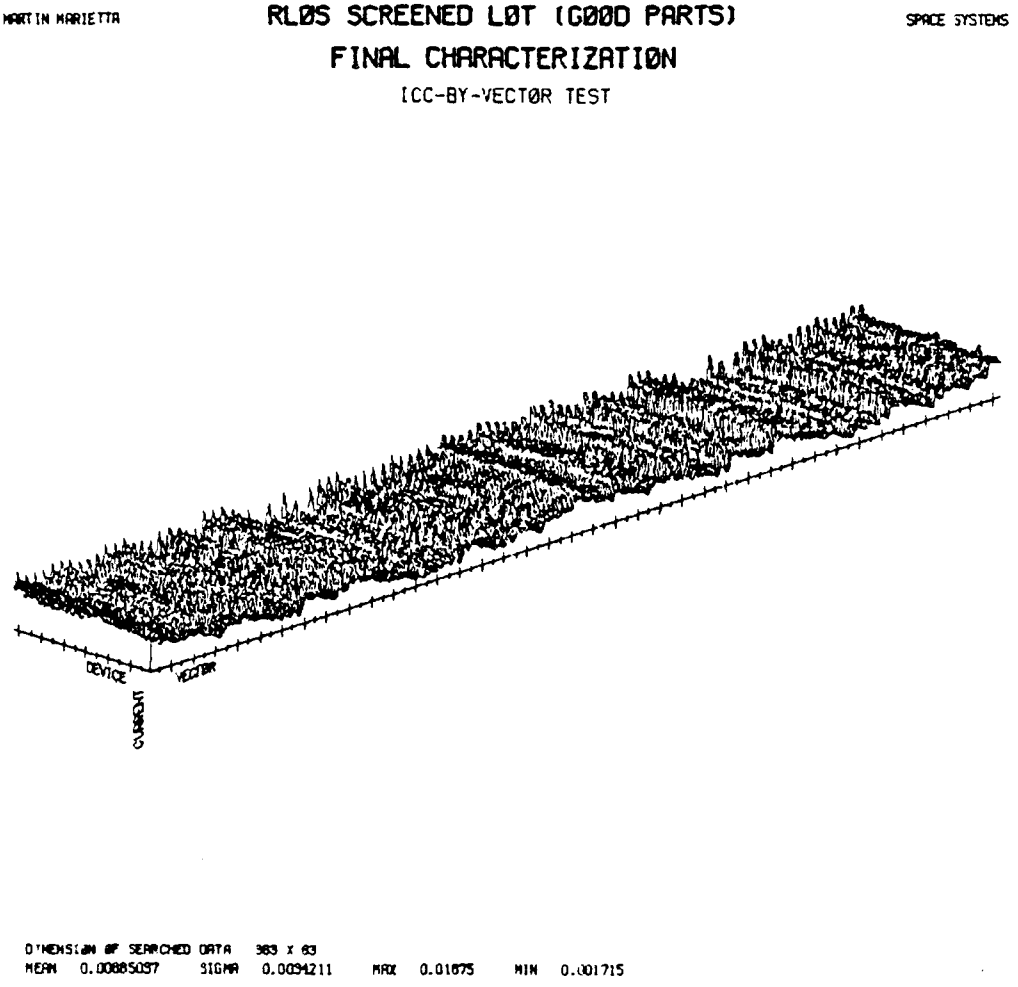

Figure 137 Overview of ICC vs Test Vector, Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

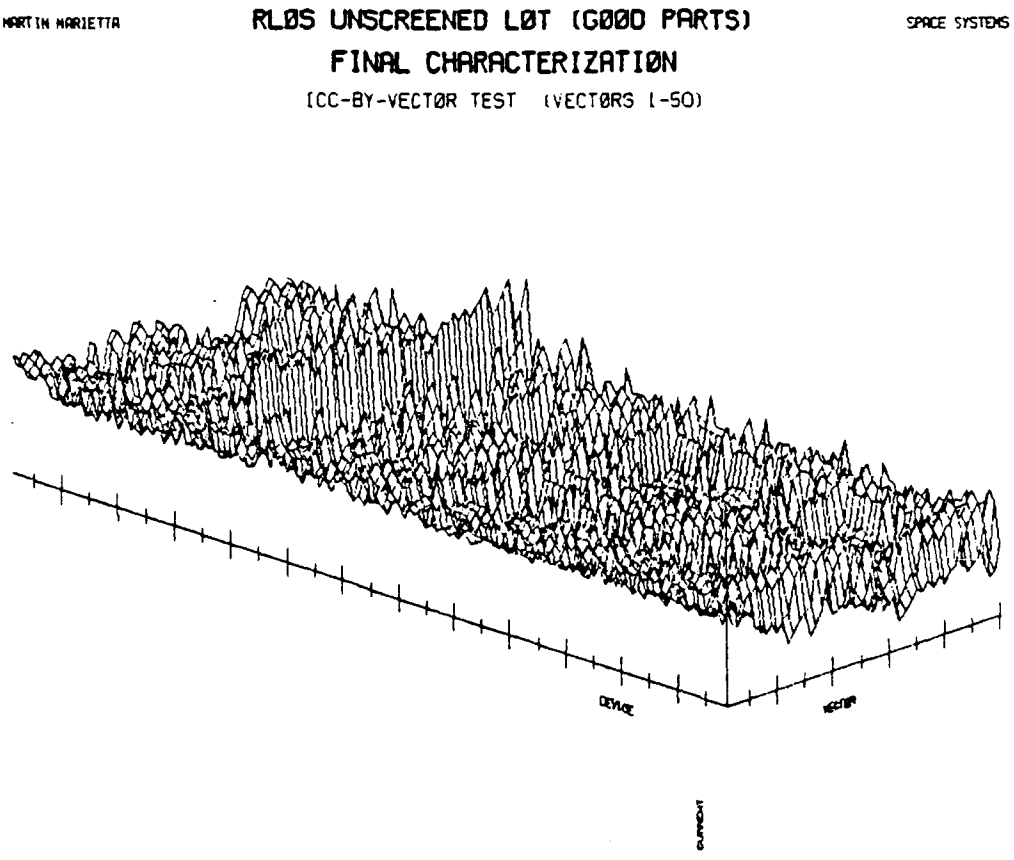

Figure 138 ICC vs Test Vector (1-50), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

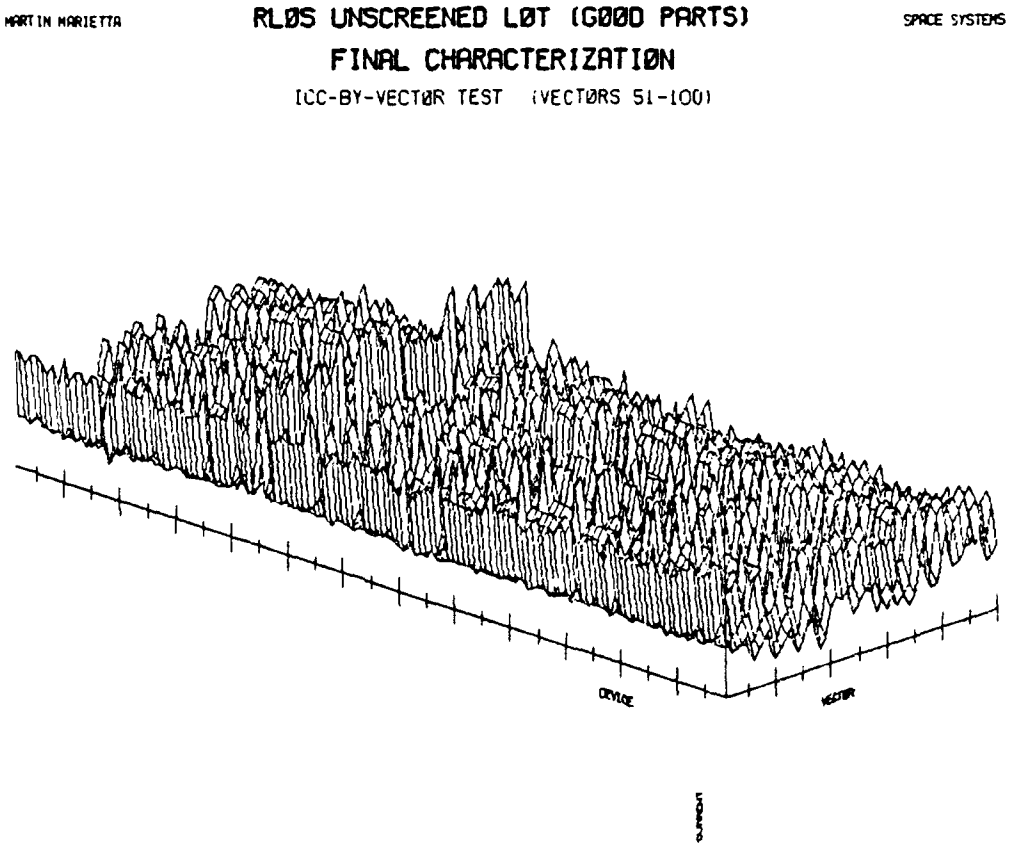

Figure 139 ICC vs Test Vector (51-100), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

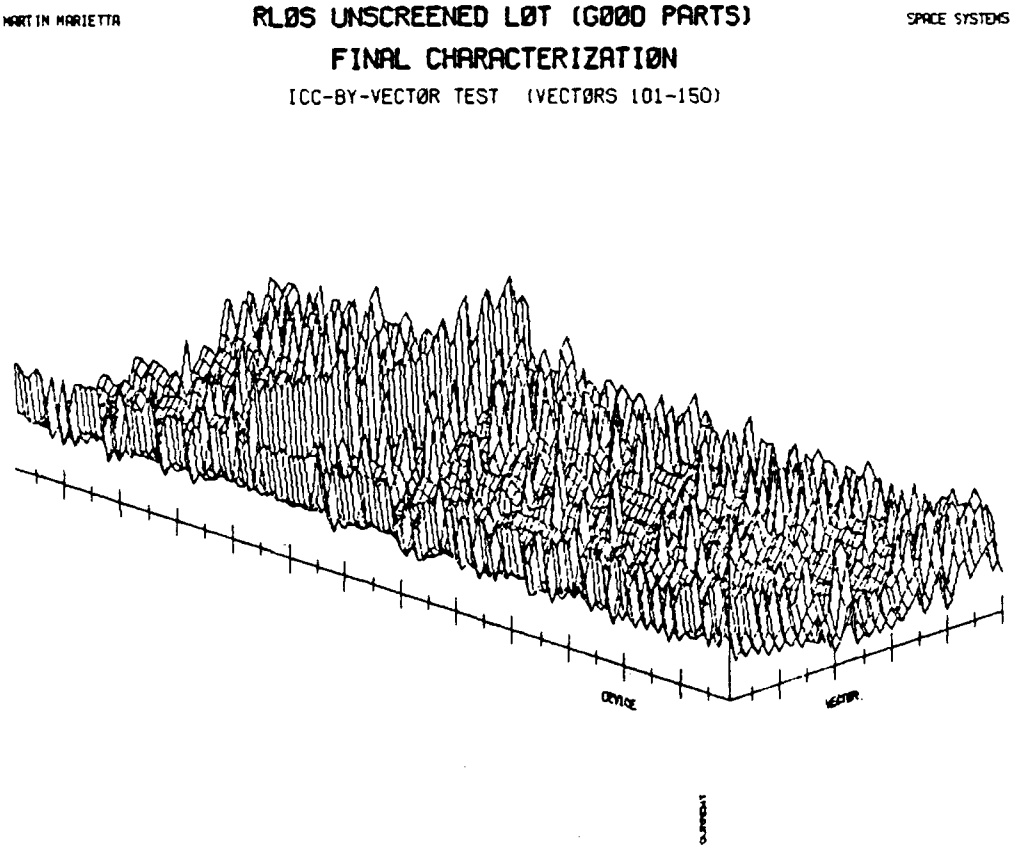

Figure 140 ICC vs Test Vector (101-150), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

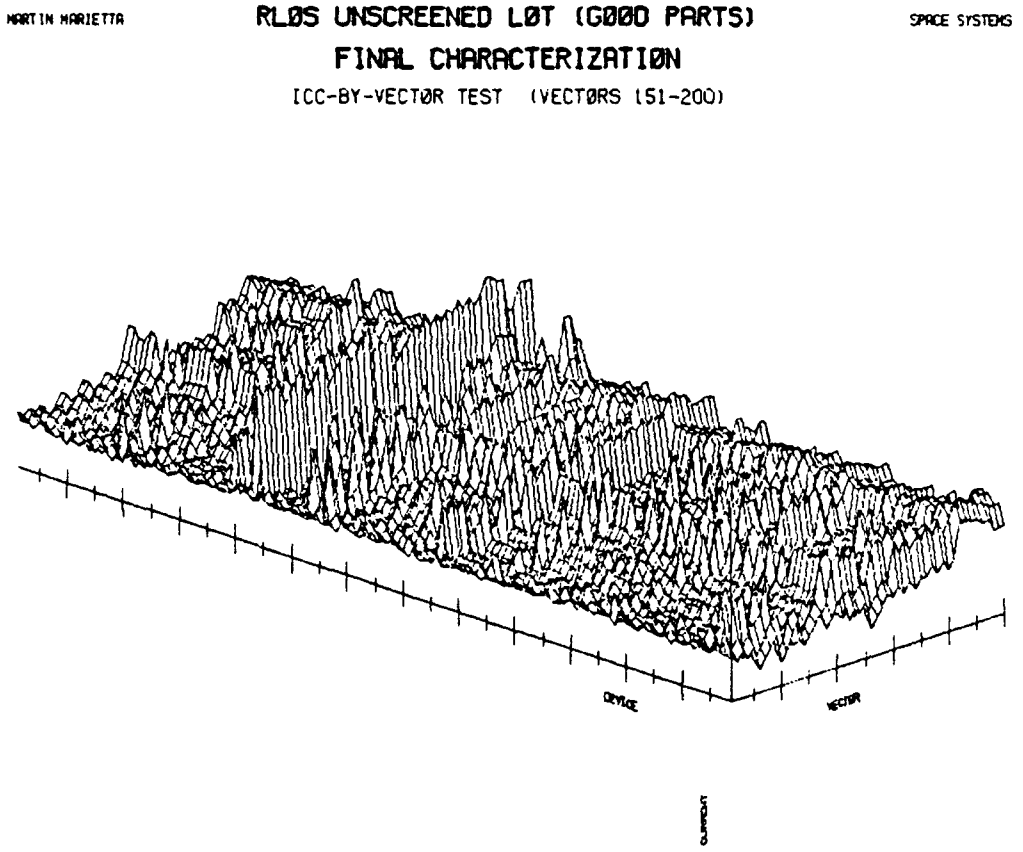

Figure 141 ICC vs Test Vector (151-200), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

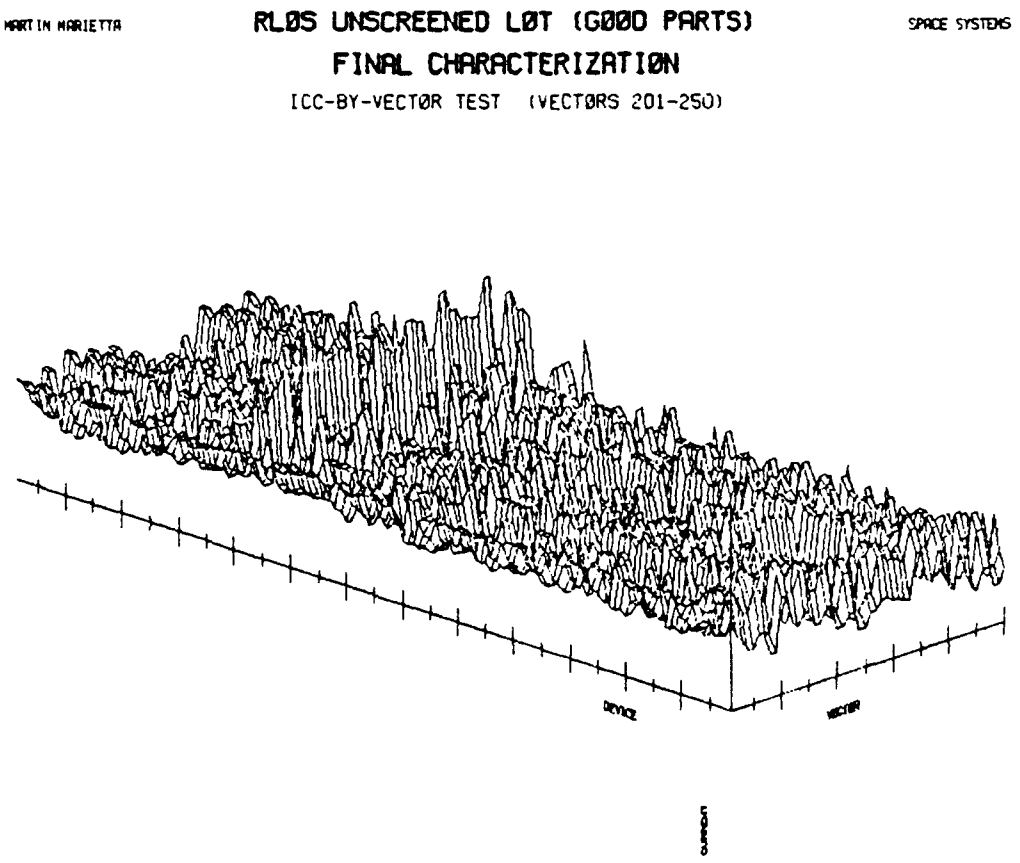

Figure 142 ICC vs Test Vector (201-250), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

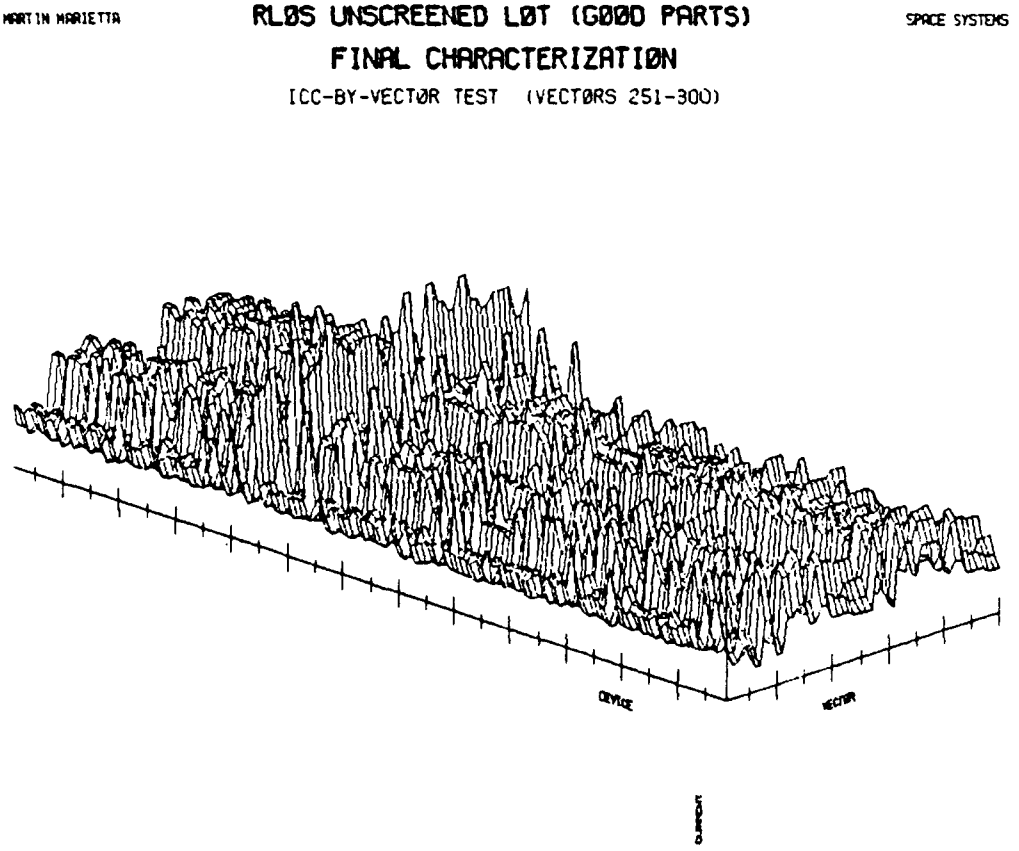

Figure 143 ICC vs Test Vector (251-300), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

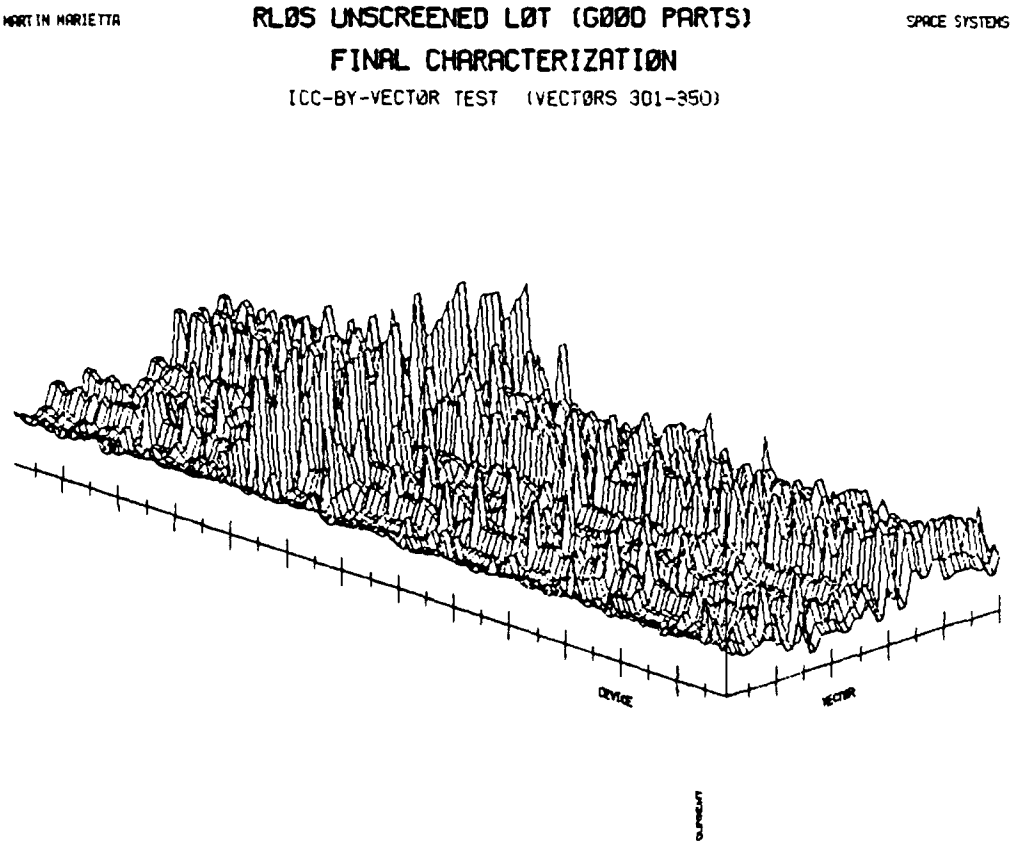

Figure 144 ICC vs Test Vector (301-350), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

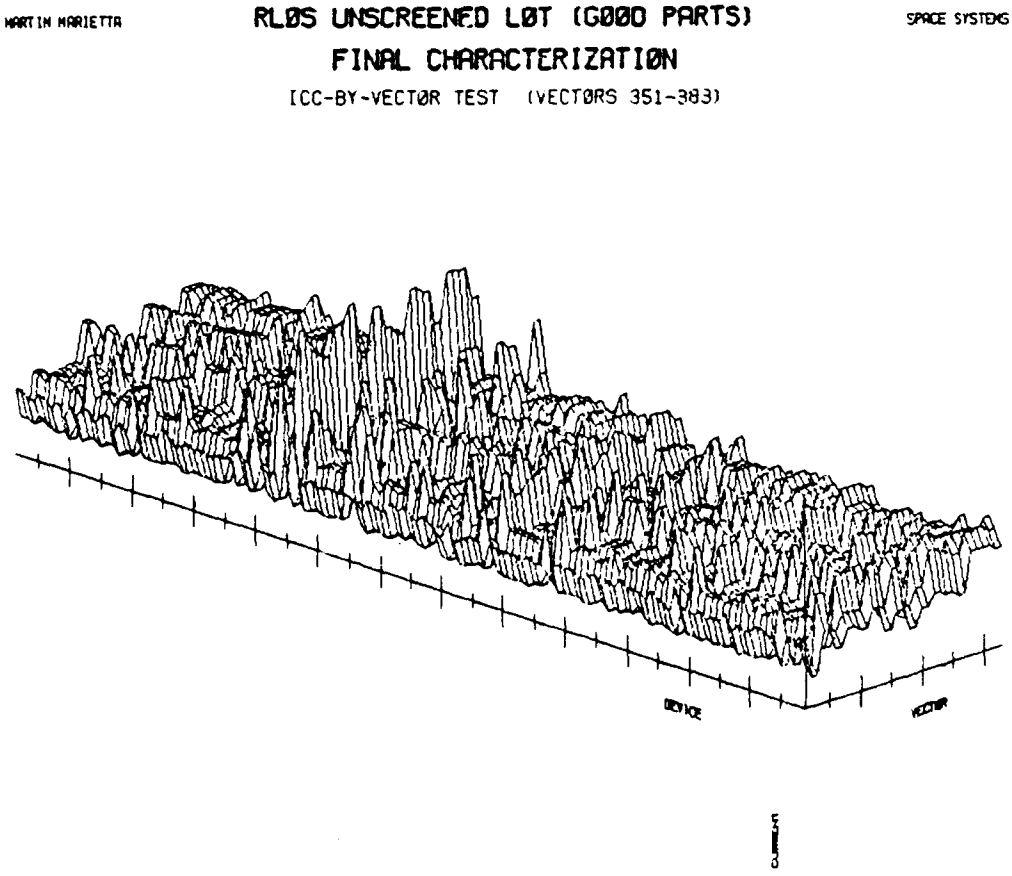

Figure 145 ICC vs Test Vector (351-383), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-129
Z-Axis: ICC 0-30 mA

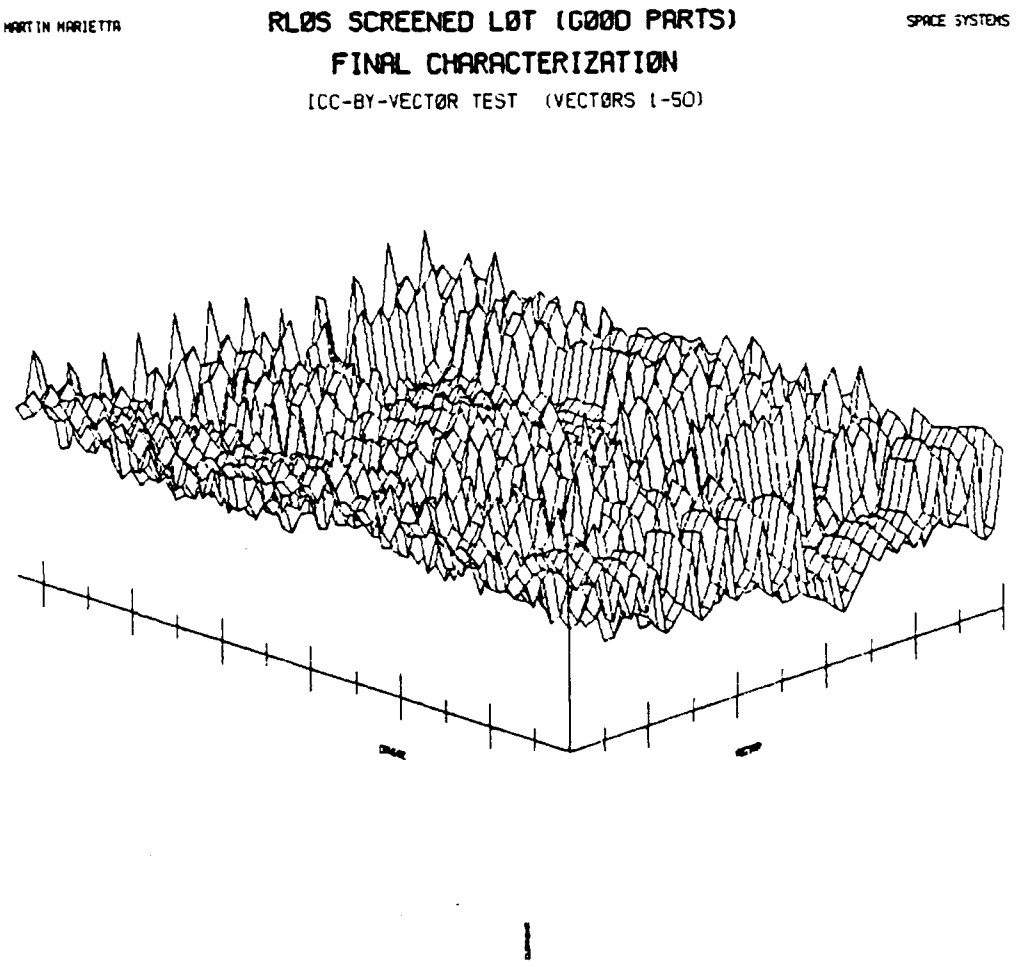

Figure 146 ICC vs Test Vector (1-50), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

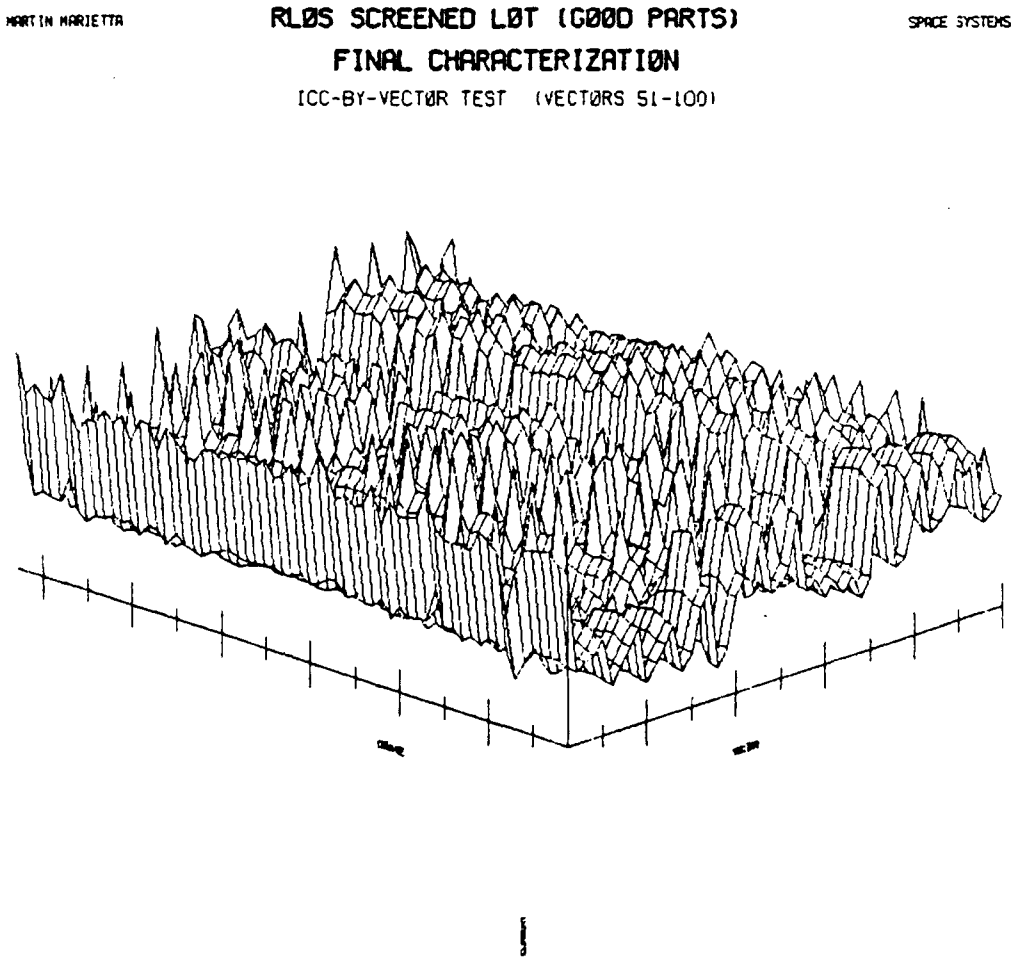

Figure 147 ICC vs Test Vector (51-100), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

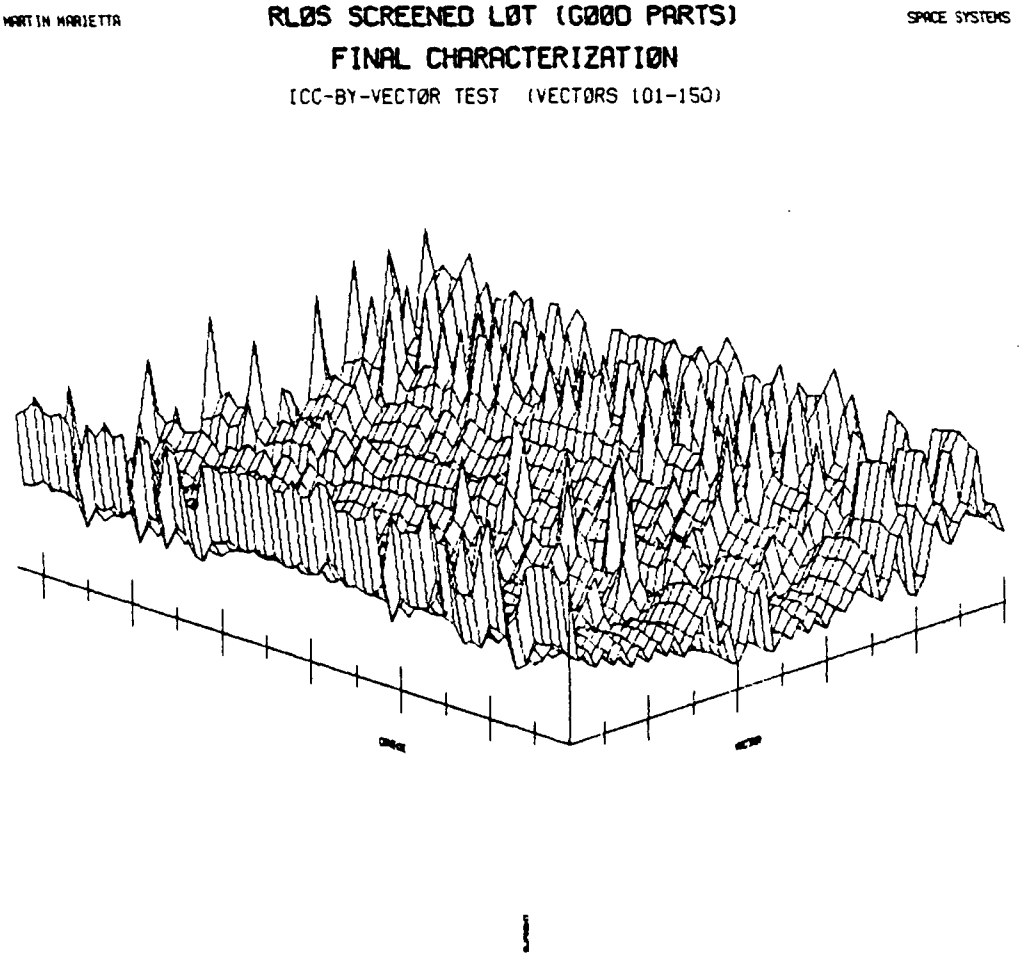

Figure 148 ICC vs Test Vector (101-150), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

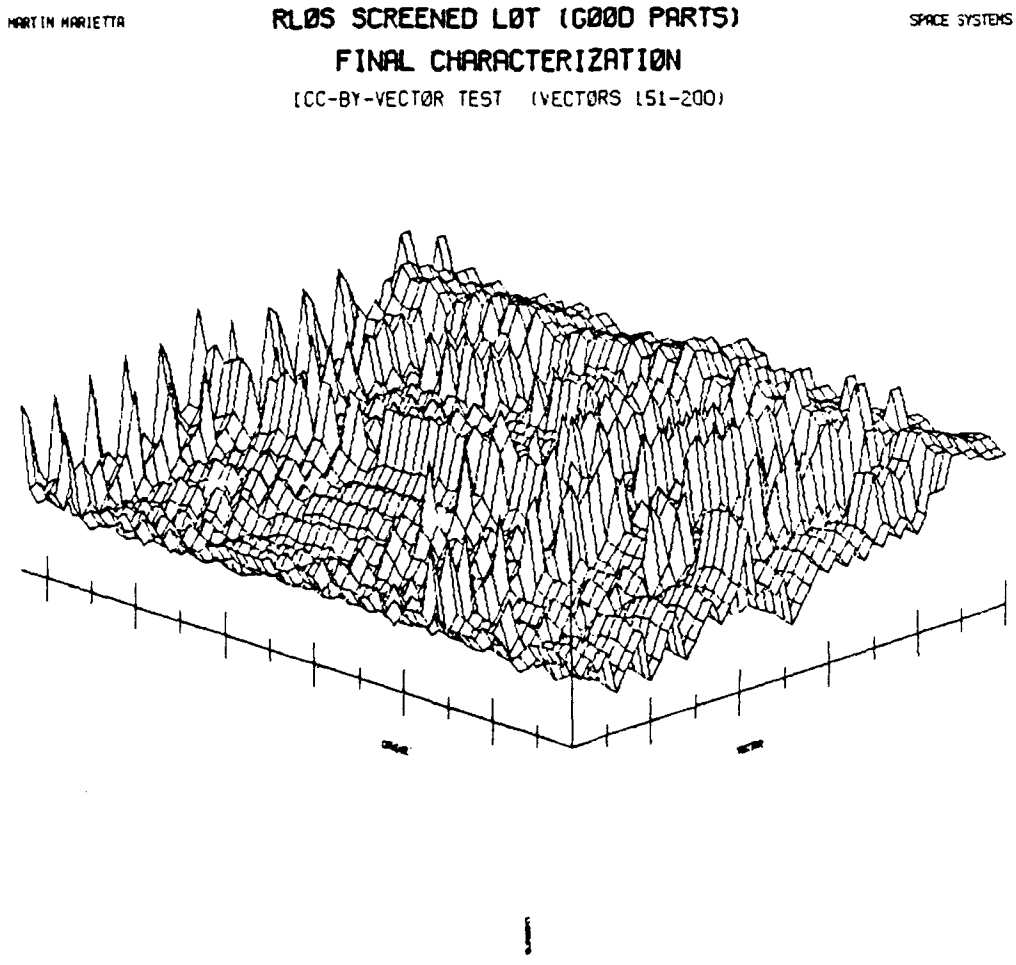

Figure 149 ICC vs Test Vector (151-200), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

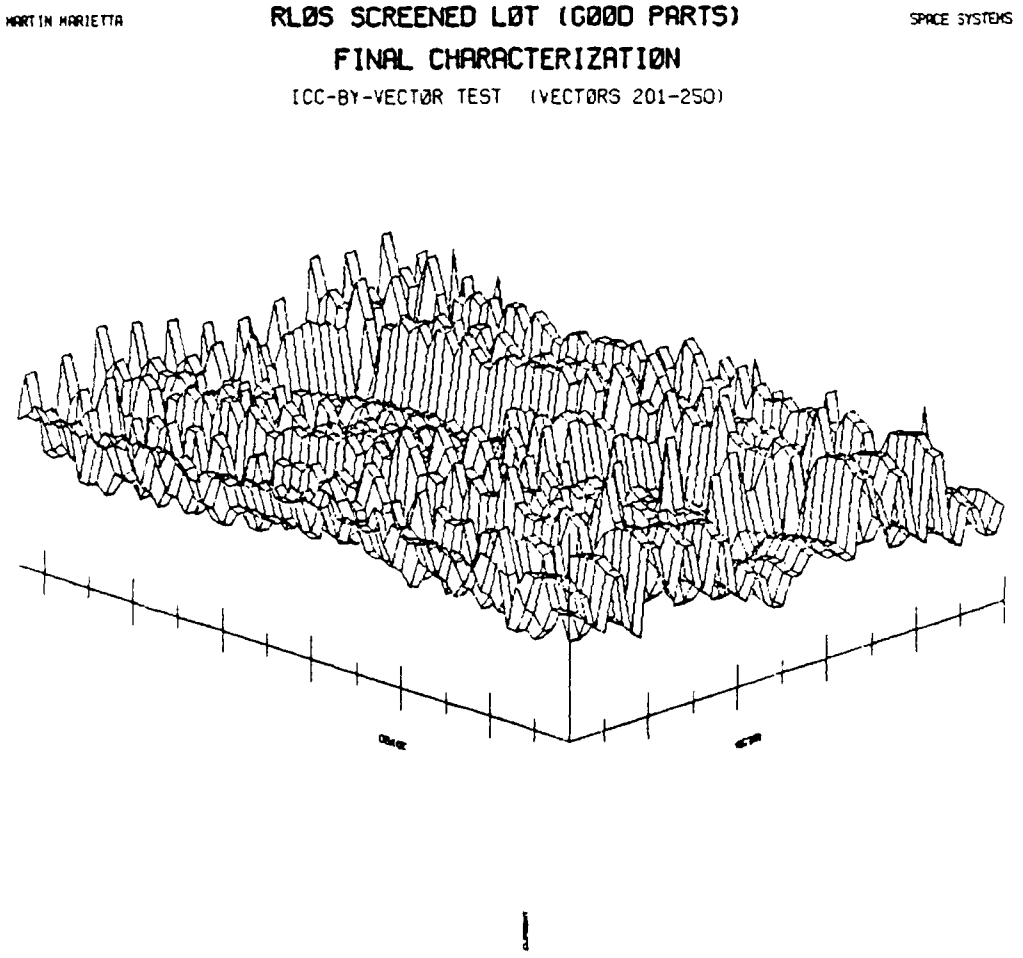

Figure 150 ICC vs Test Vector (201-250), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-63
Z Axis: ICC 0-20 mA

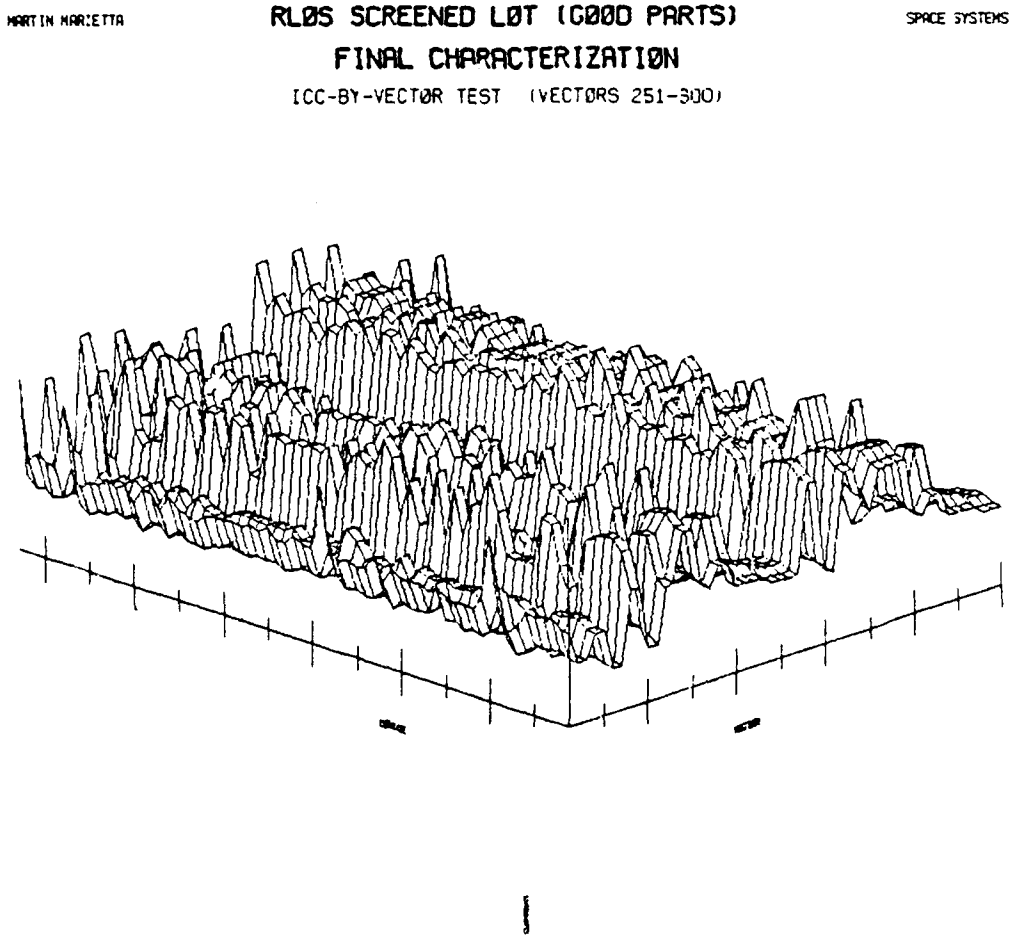

Figure 151 ICC vs Test Vector (251-300), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

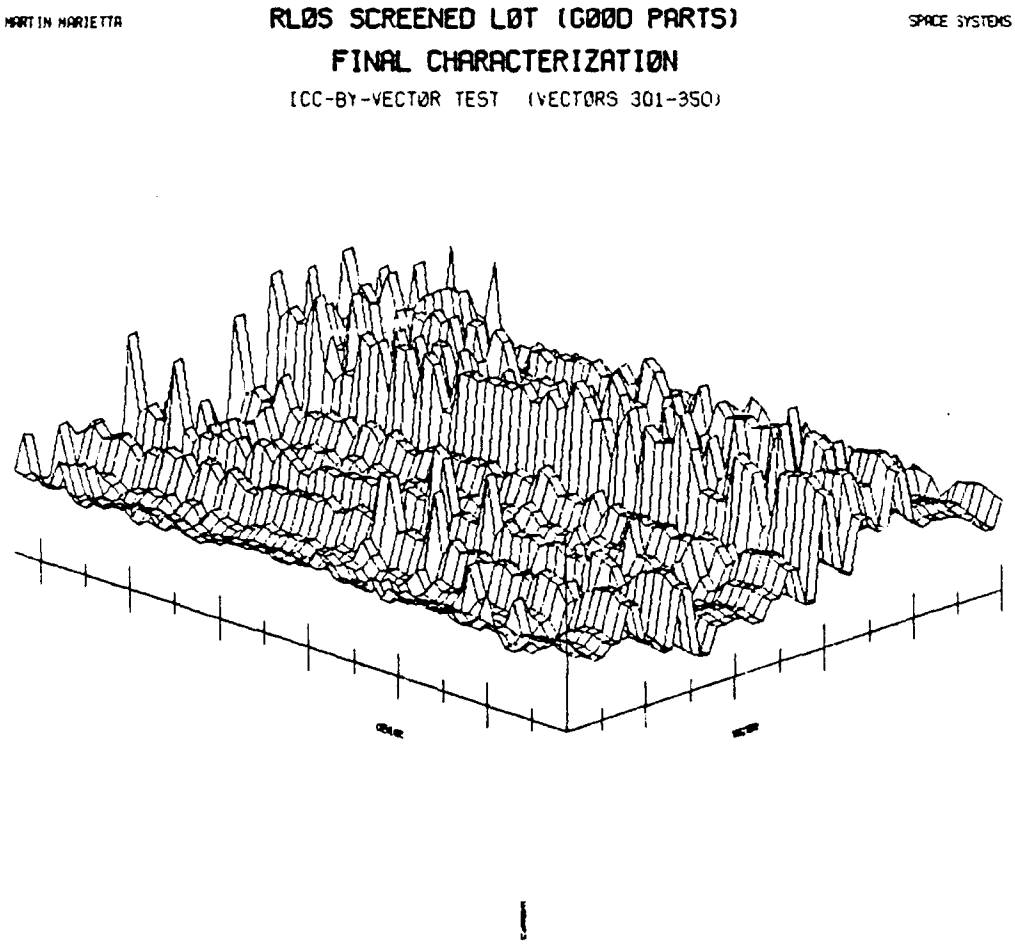

Figure 152 ICC vs Test Vector (301-350), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

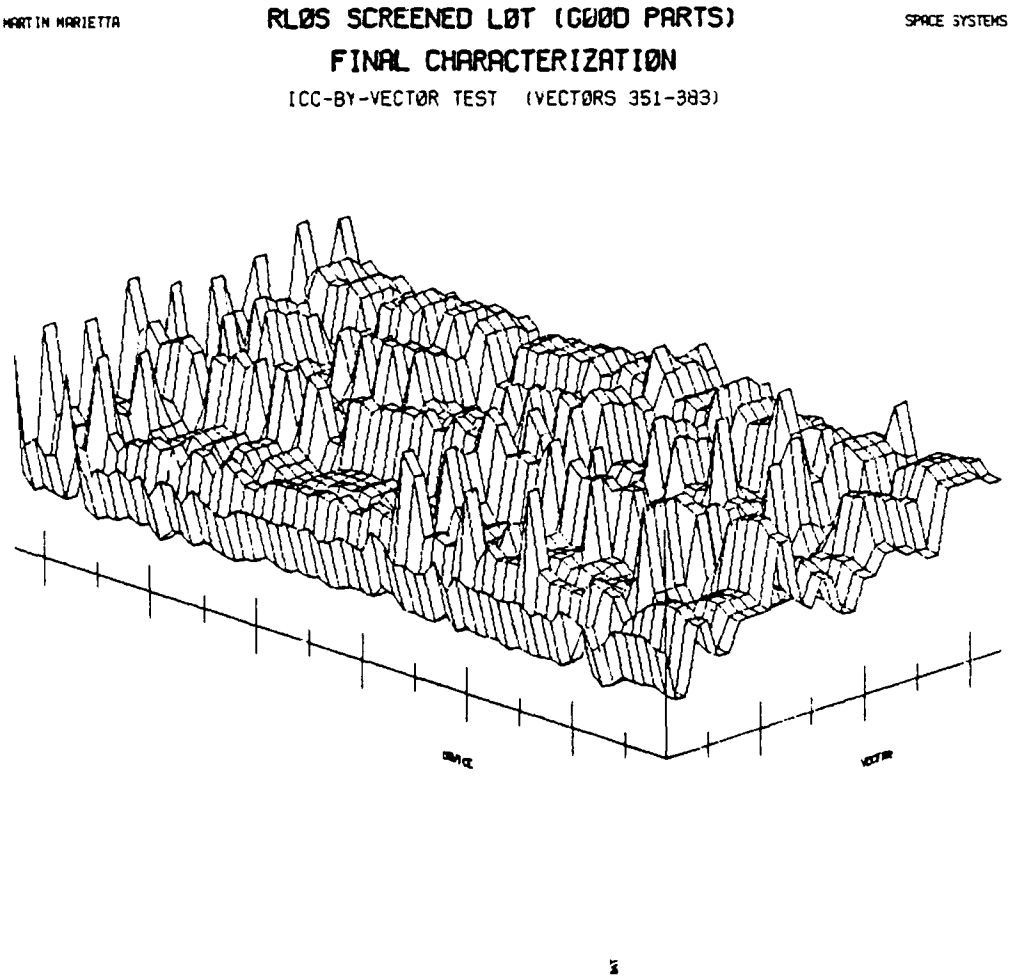

Figure 153 ICC vs Test Vector (351-383), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-63
Z-Axis: ICC 0-20 mA

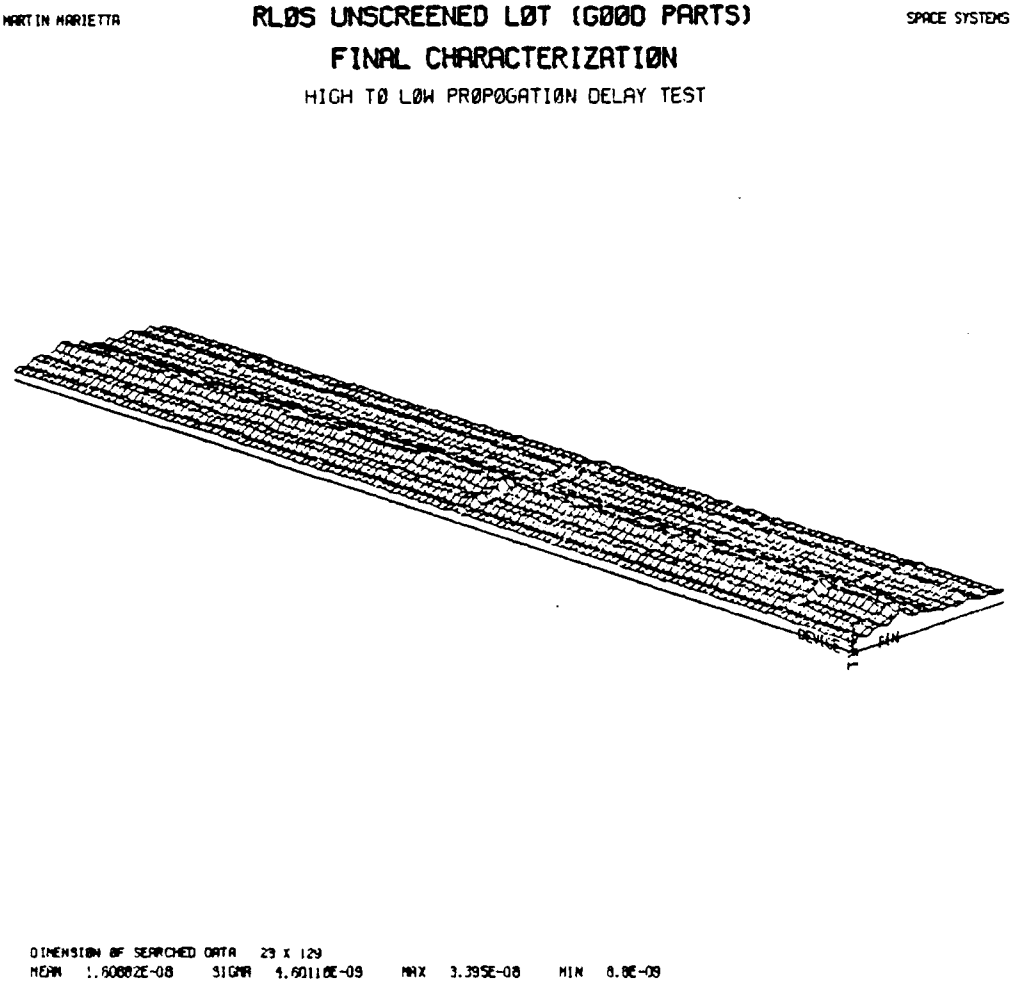

Figure 154 High to Low Propagation Delays, Unscreened Lot, Final Data

Plot Information:

X-Axis: Pins 1-23
Y-Axis: Devices 1-129
Z-Axis: Tphl 0-35 nS

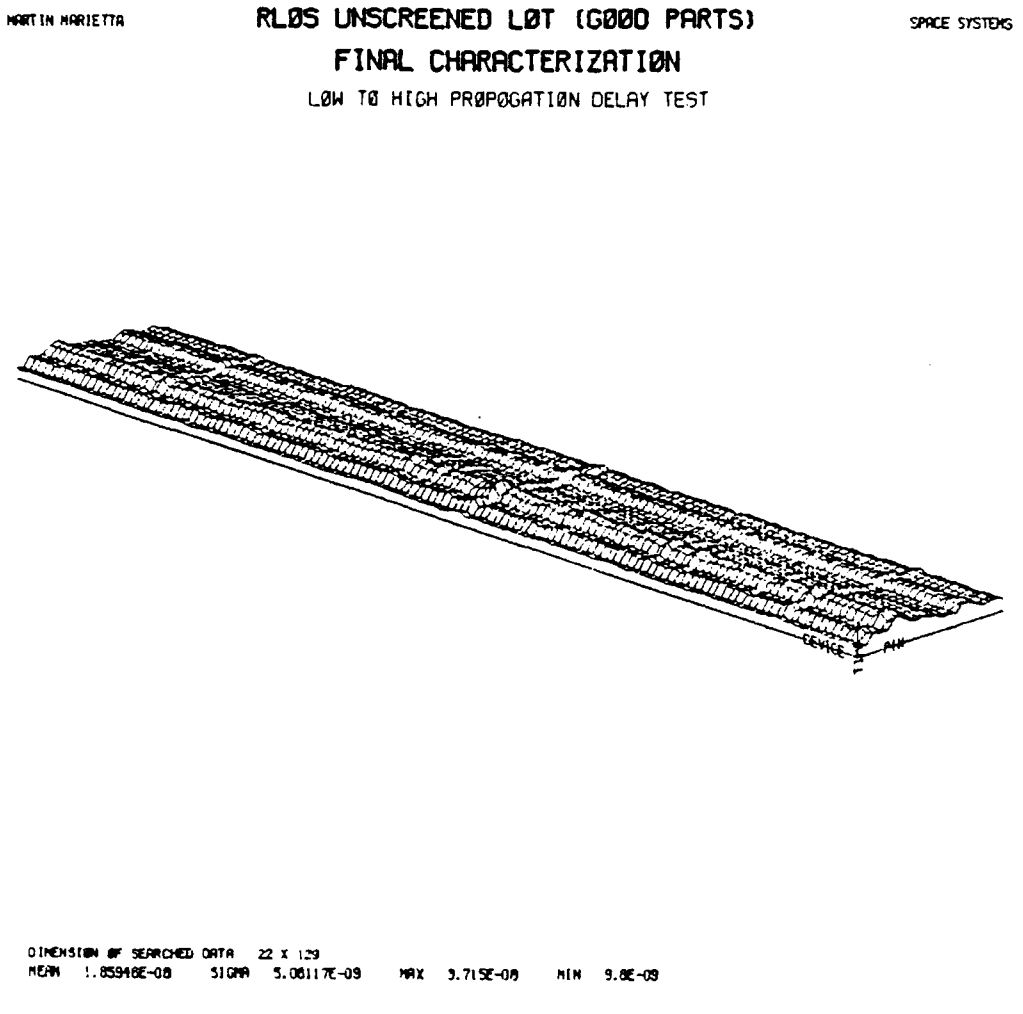

Figure 155 Low to High Propagation Delays, Unscreened Lot, Final Data

Plot Information:

X-Axis: Pins 1-22
Y-Axis: Devices 1-129
Z-Axis: Tplh 0-40 nS

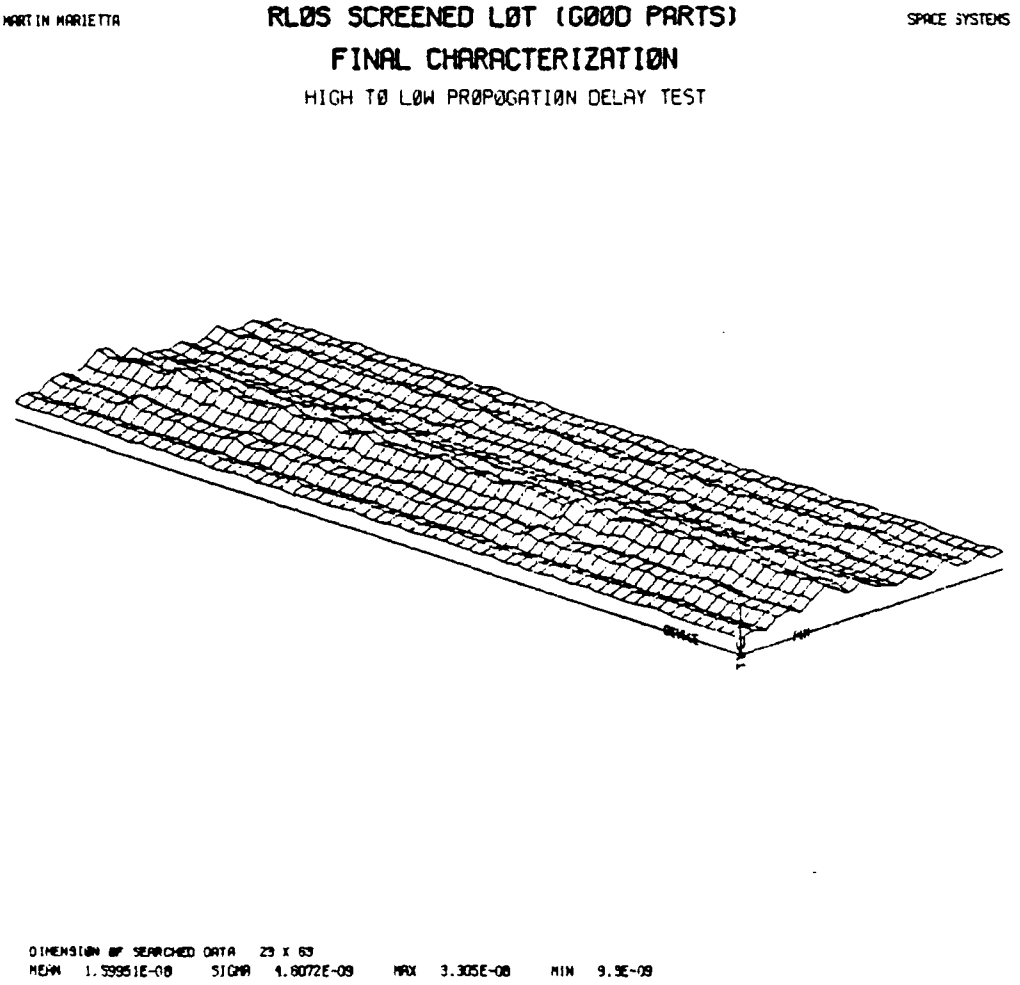

Figure 156 High to Low Propagation Delays, Screened Lot, Final Data

Plot Information:

X-Axis: Pins 1-23
Y-Axis: Devices 1-63
Z-Axis: Tphl 0-35 nS

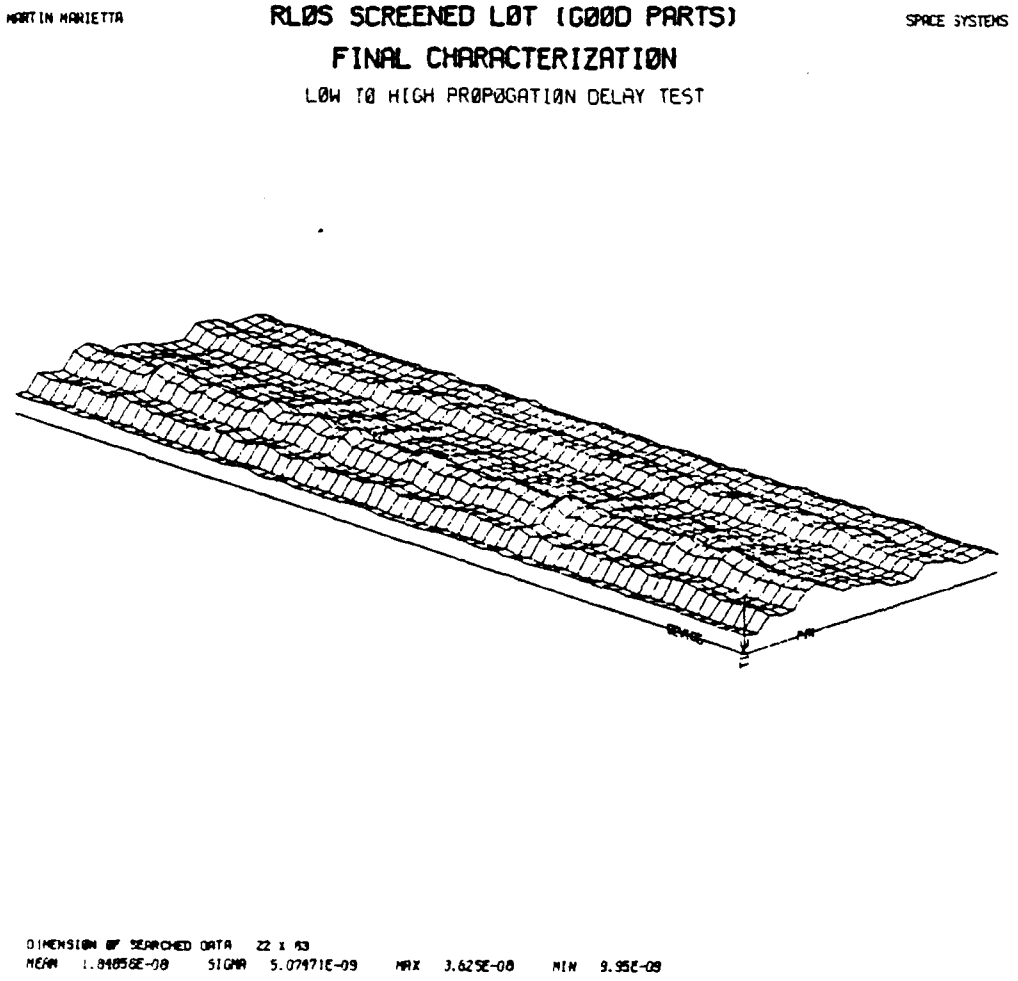

Figure 157 Low to High Propagation Delays, Screened Lot, Final Data

Plot Information:

X-Axis: Pins 1-22
Y-Axis: Devices 1-63
Z-Axis: Tplh 0-35 nS

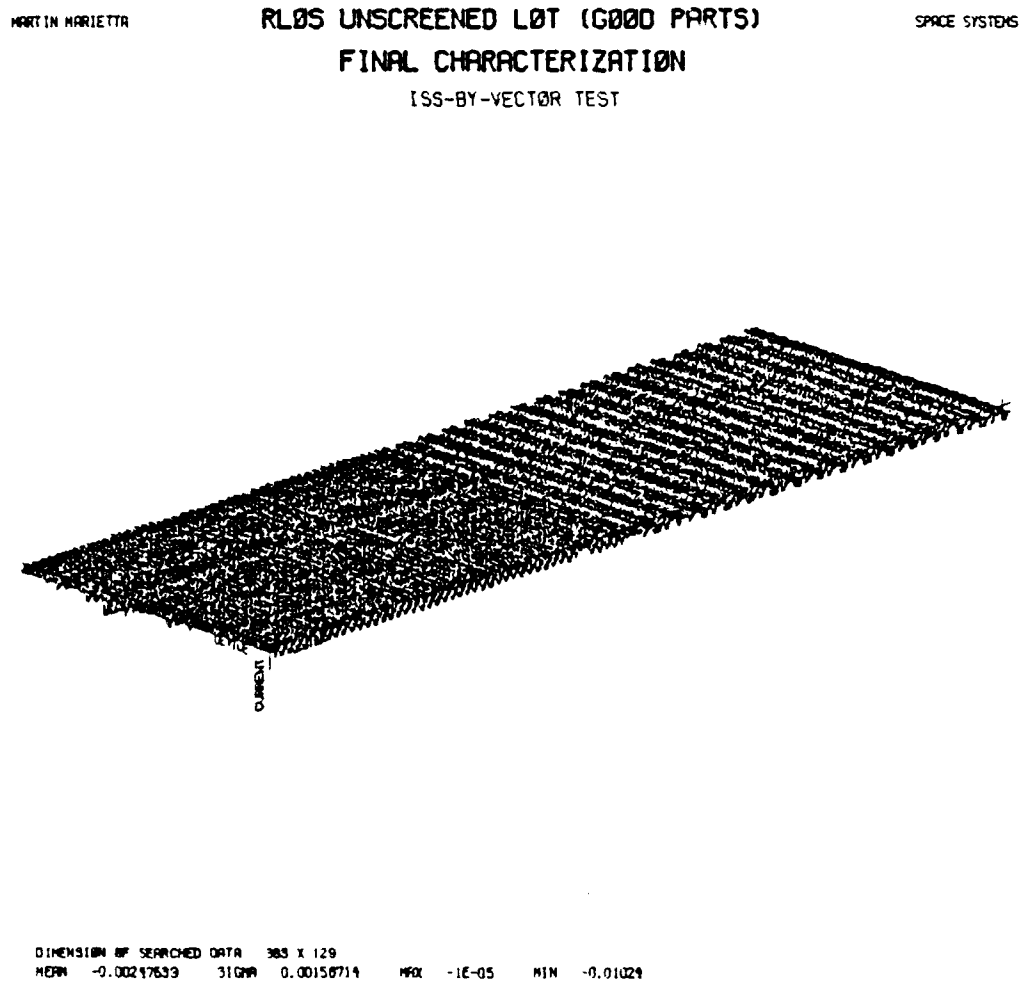

Figure 158 Overview of ISS vs Test Vector, Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

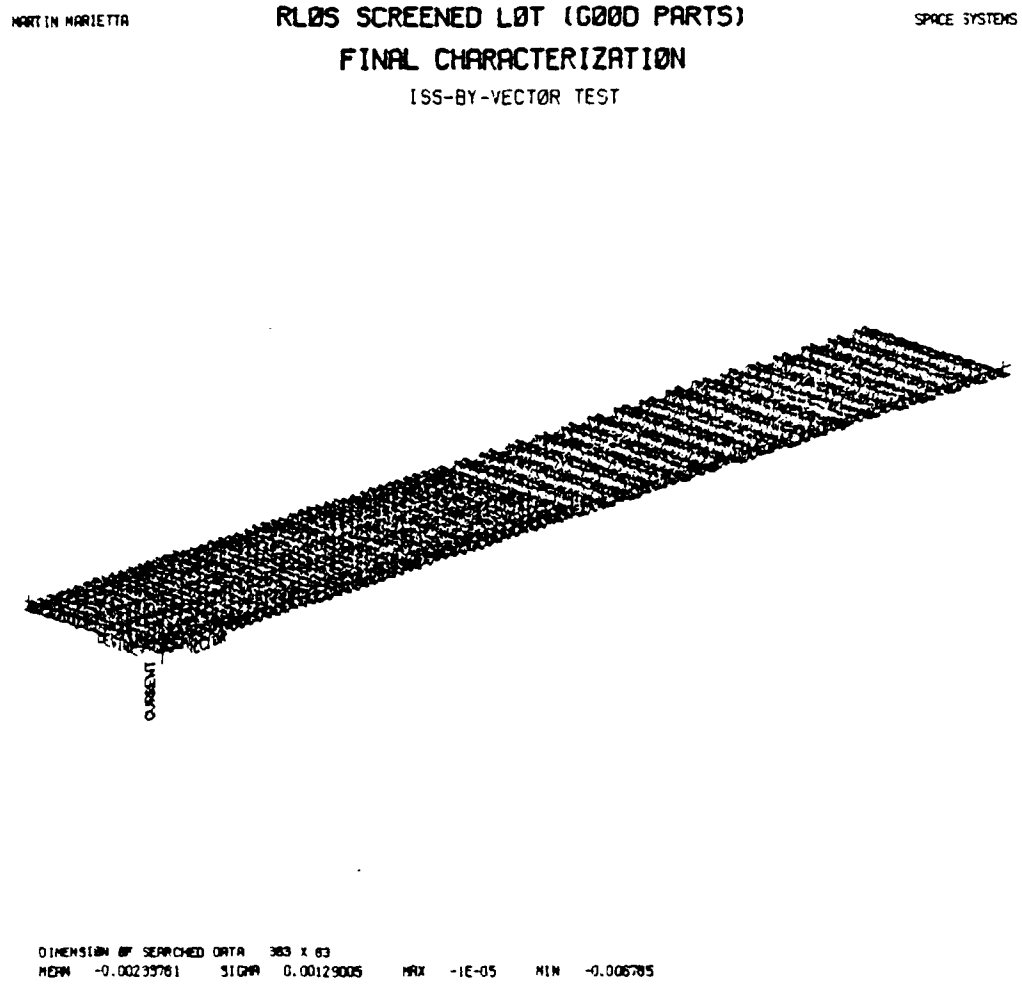

Figure 159 Overview of ISS vs Test Vector, Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-383
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

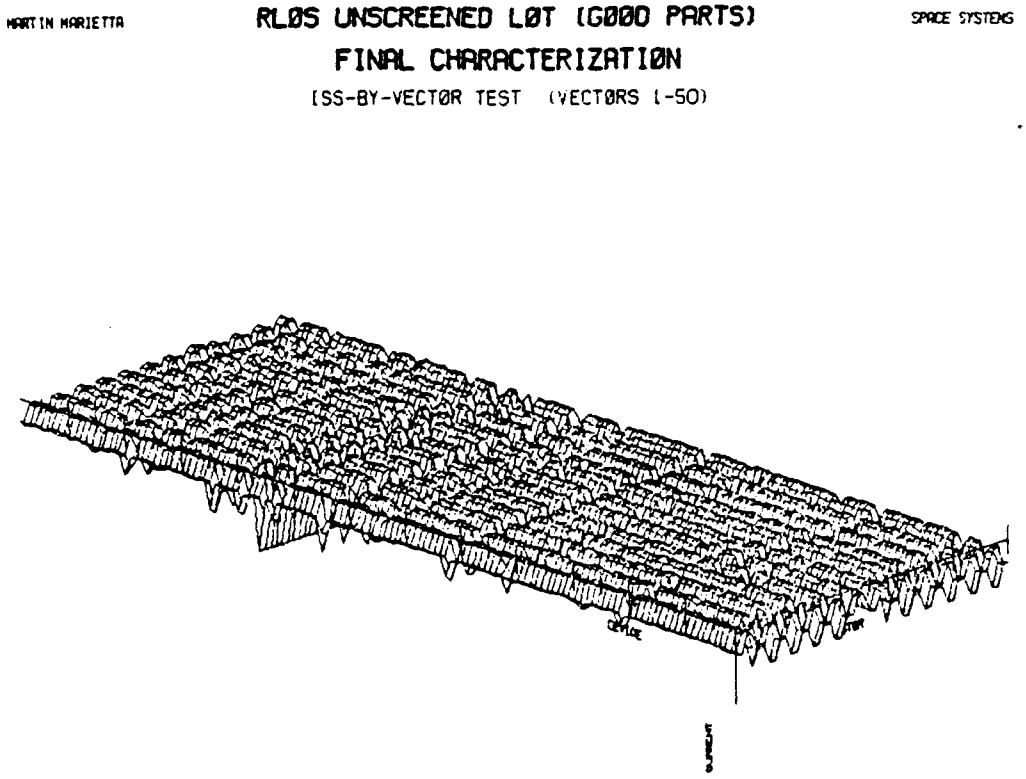

Figure 160 ISS vs Test Vector (1-50), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

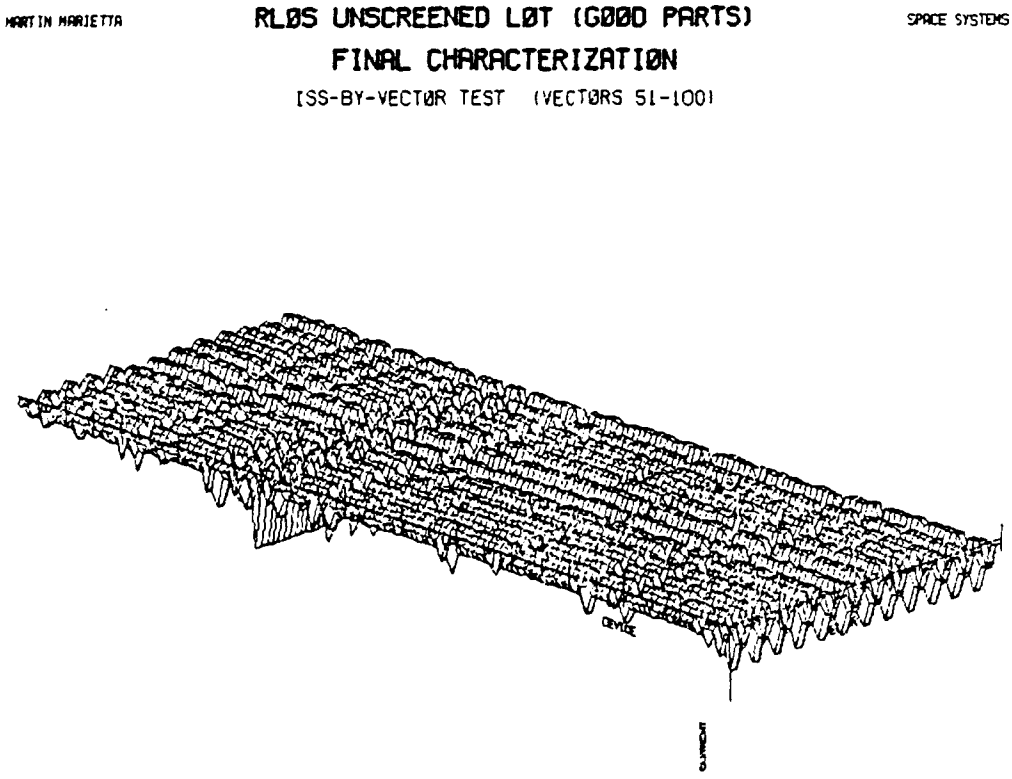

Figure 161 ISS vs Test Vector (51-100), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

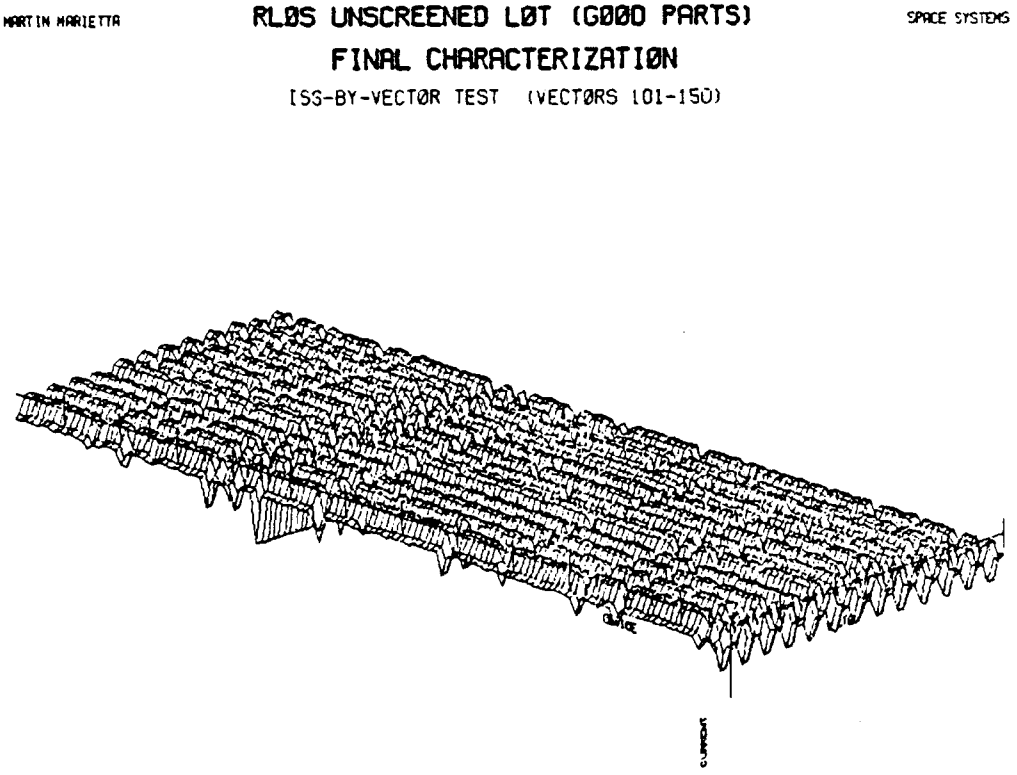

Figure 162 ISS vs Test Vector (101-150), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

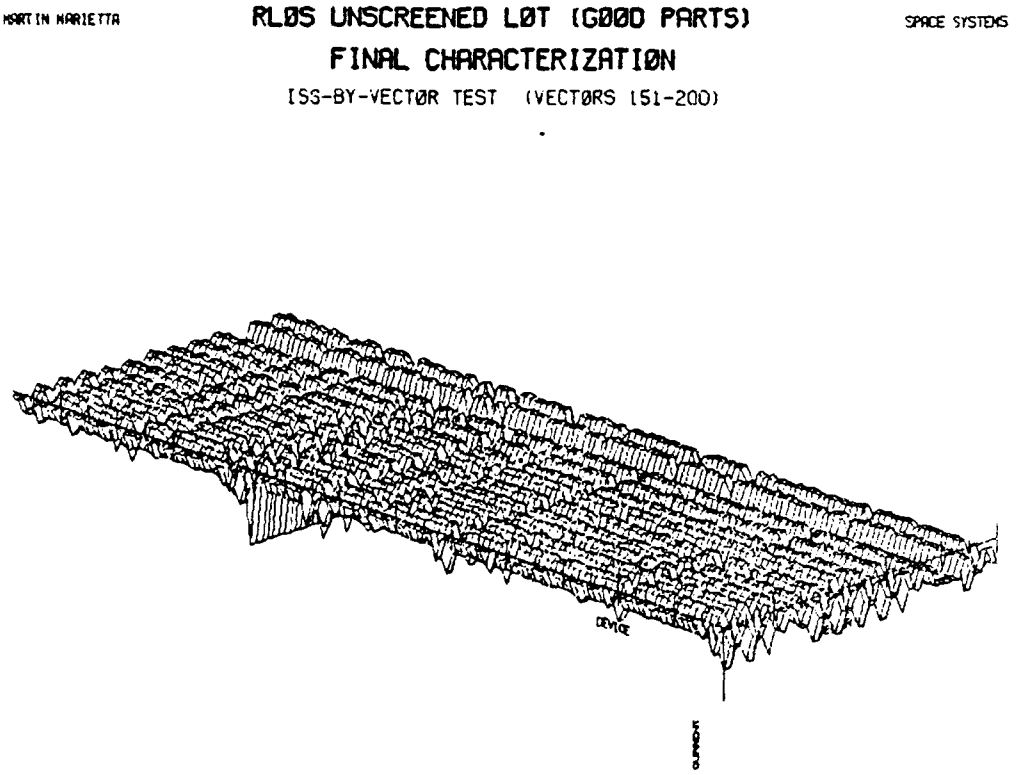

Figure 163 ISS vs Test Vector (151-200), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

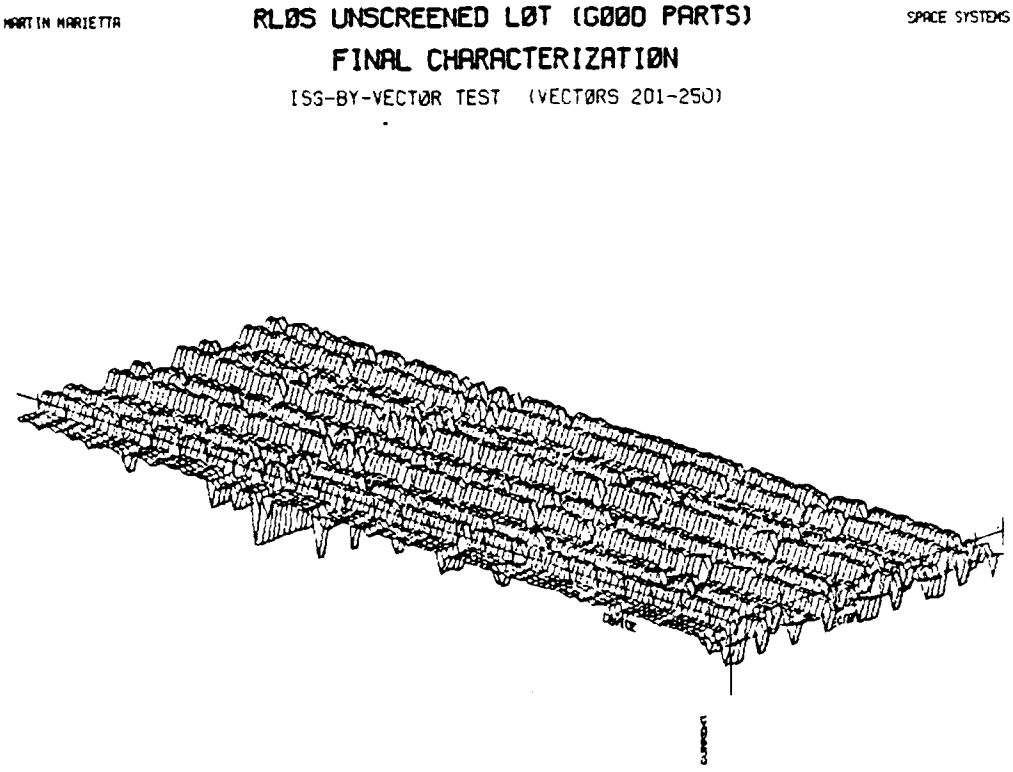

Figure 164 ISS vs Test Vector (201-250), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

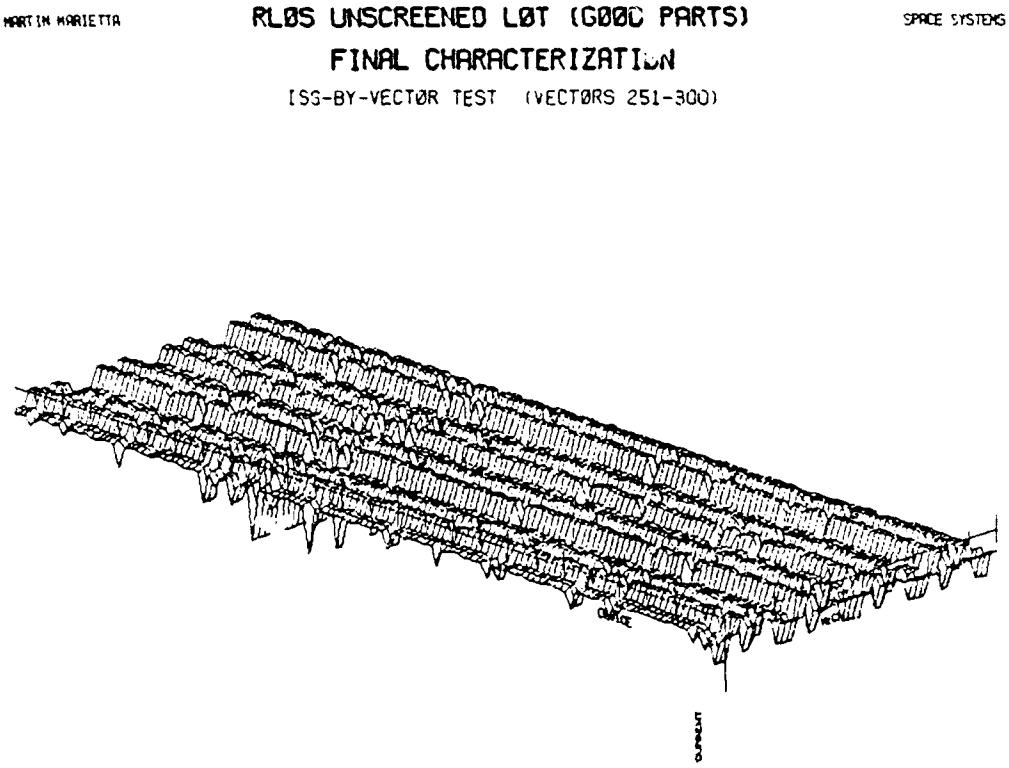

Figure 165 ISS vs Test Vector (251-300), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

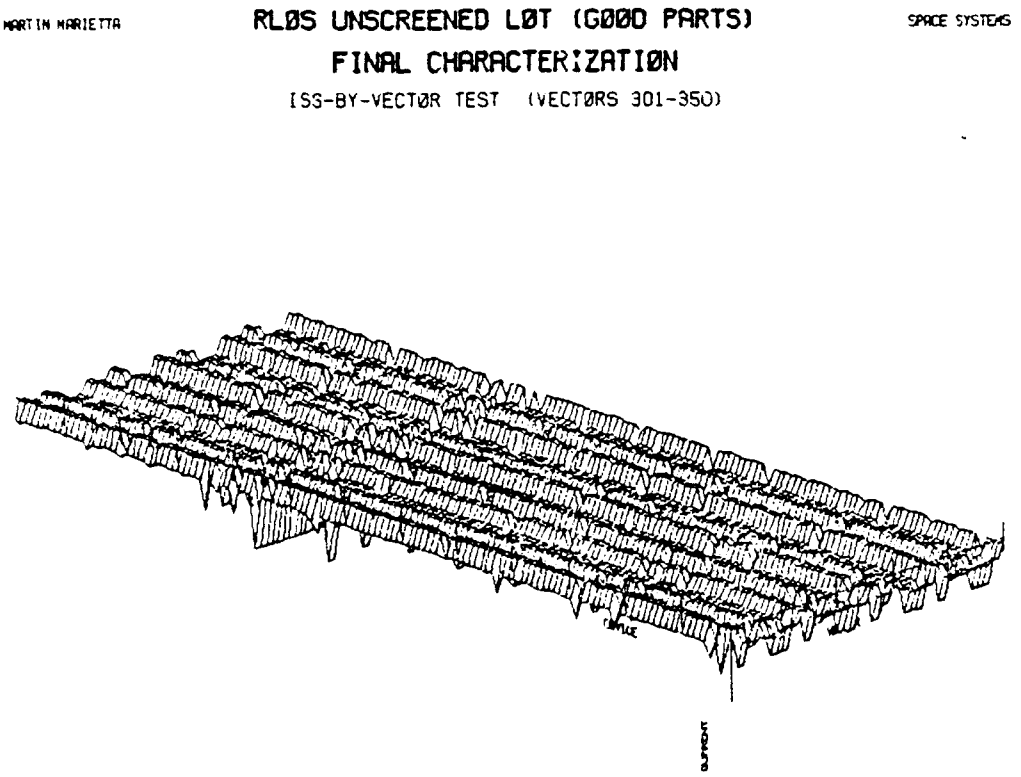

Figure 166 ISS vs Test Vector (301-350), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

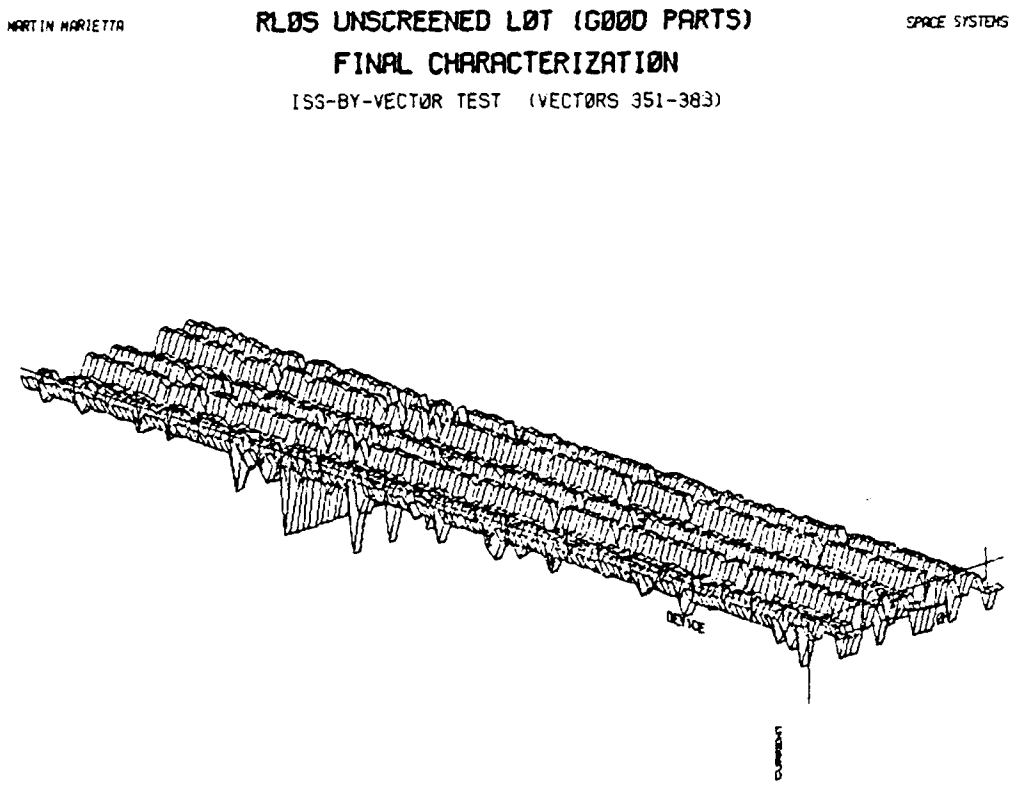

Figure 167 ISS vs Test Vector (351-383), Unscreened Lot, Final Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-129
Z-Axis: ISS -10-0 mA

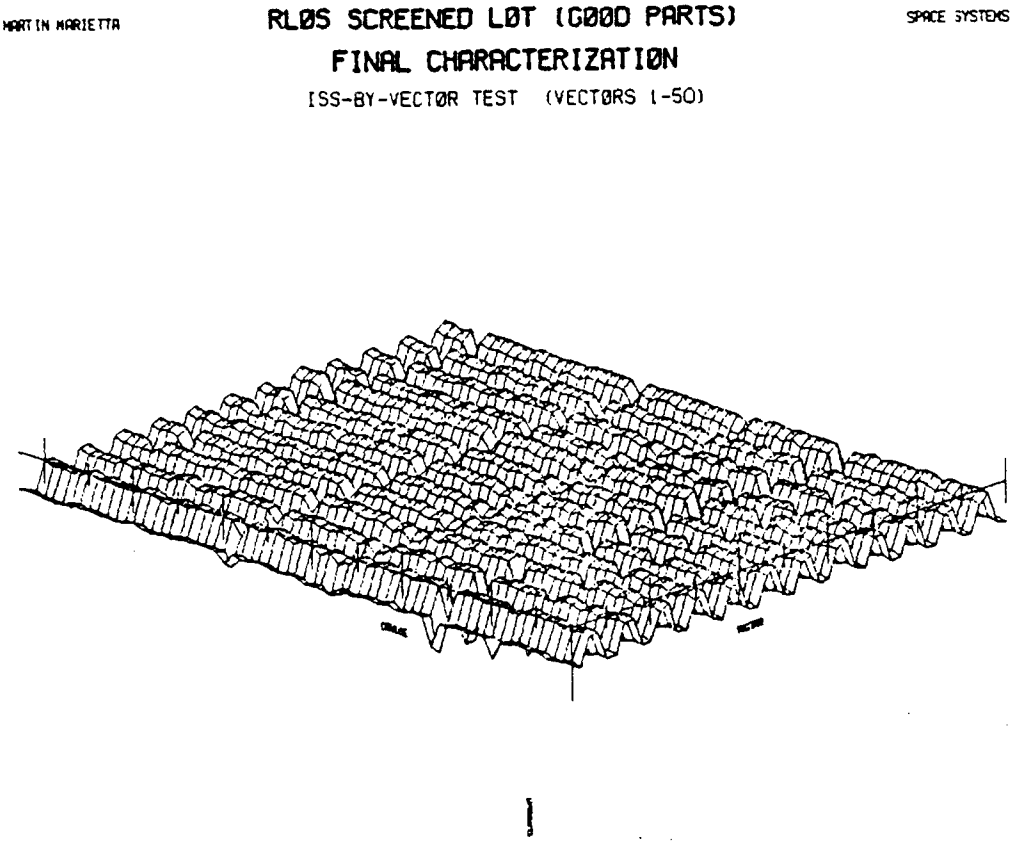

Figure 168 ISS vs Test Vector (1-50), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 1-50
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

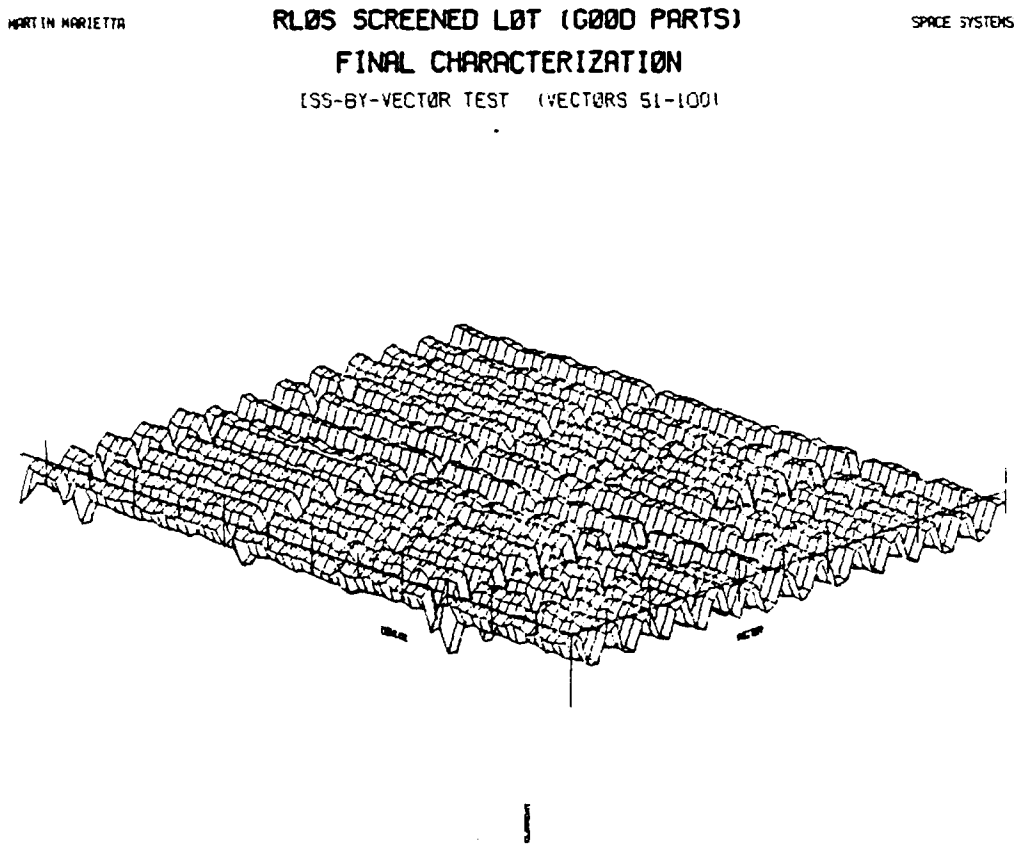

Figure 169 ISS vs Test Vector (51-100), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 51-100
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

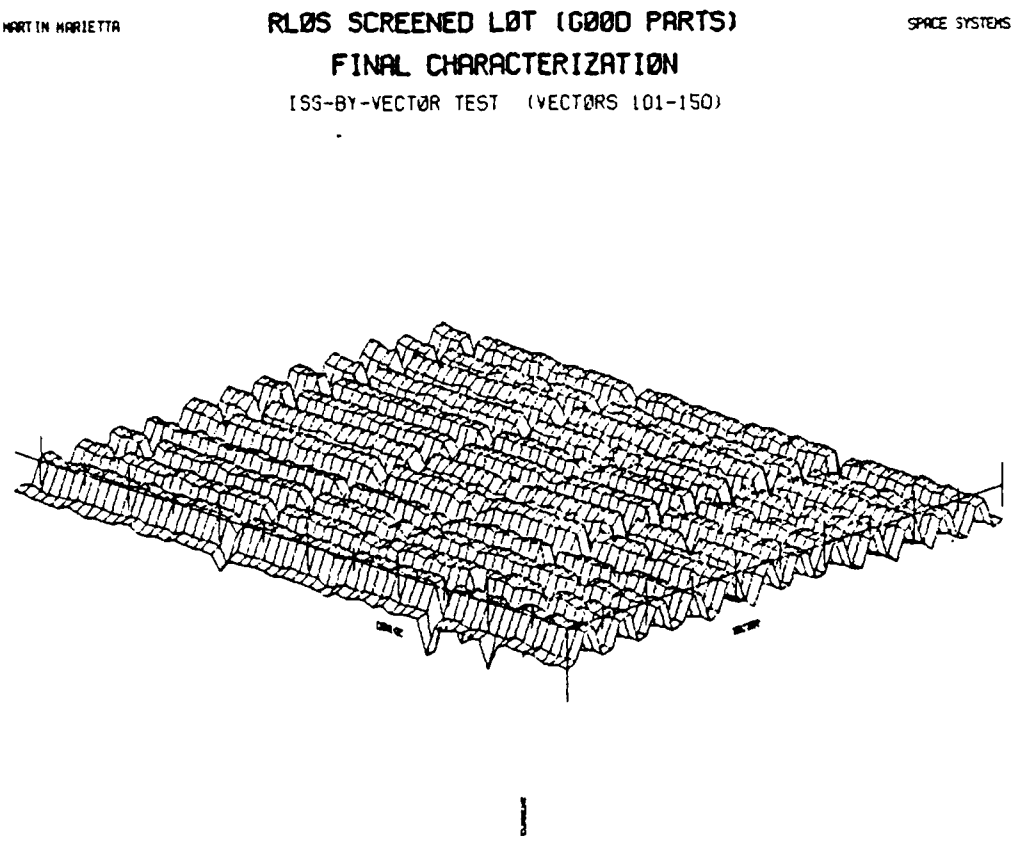

Figure 170 ISS vs Test Vector (101-150), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 101-150
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

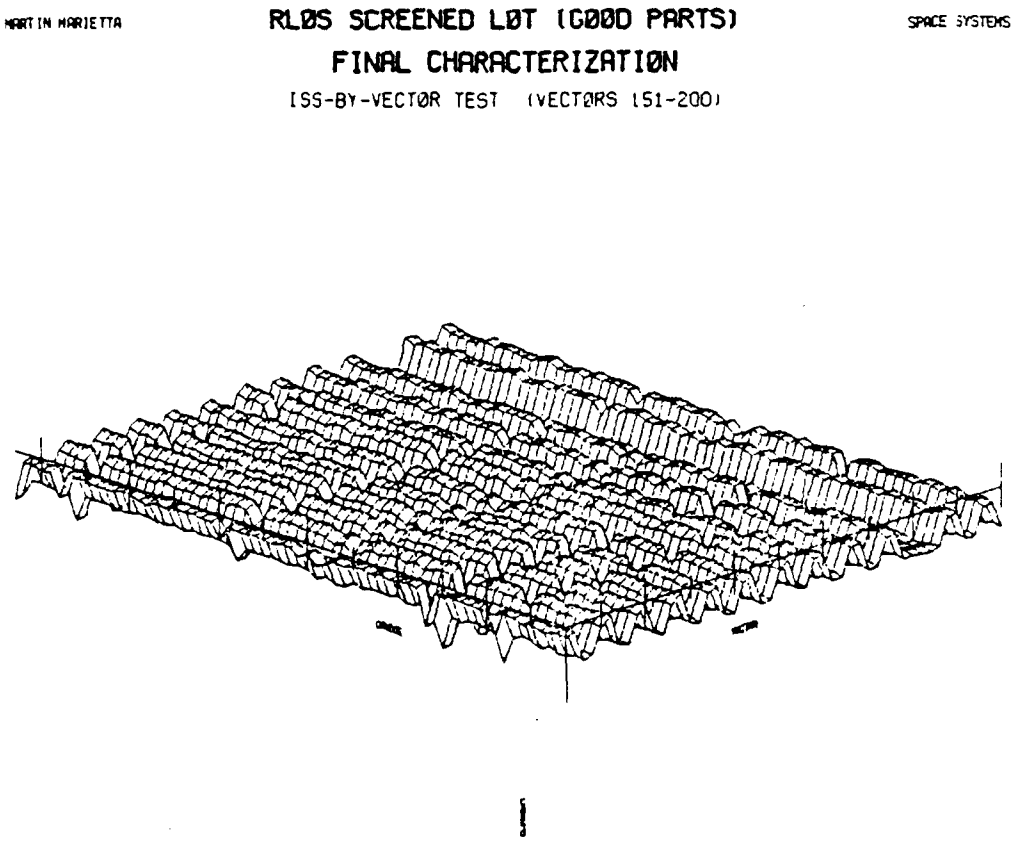

Figure 171 ISS vs Test Vector (151-200), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 151-200
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

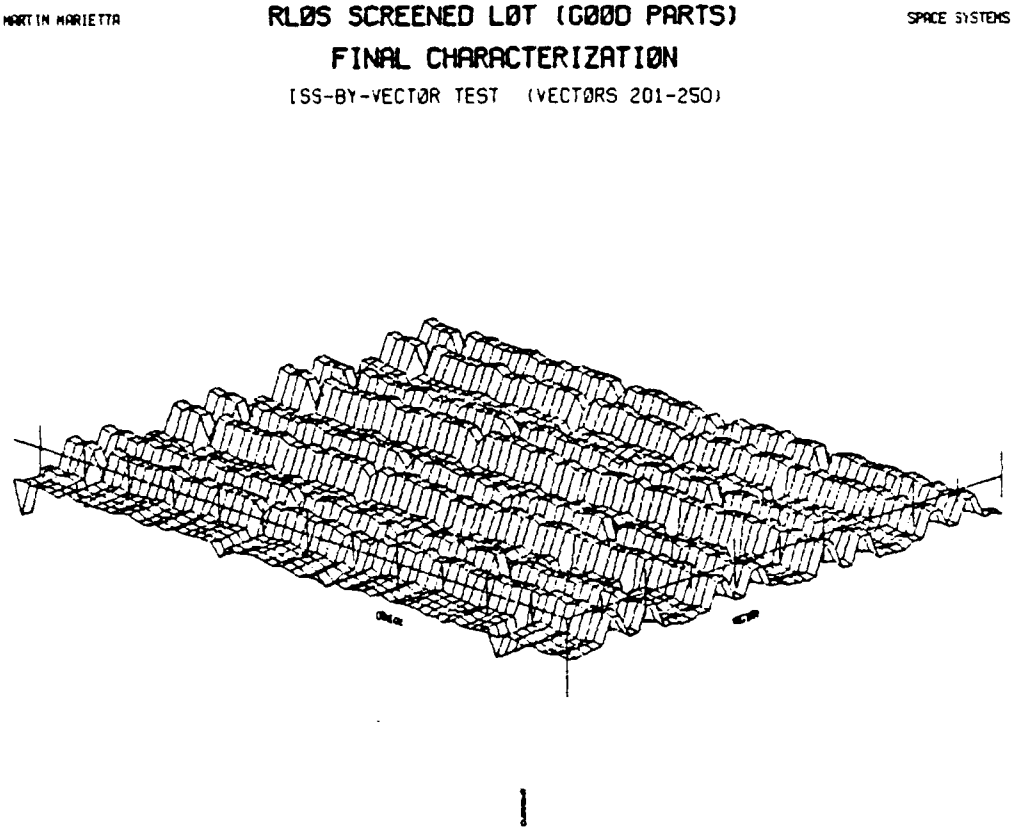

Figure 172 ISS vs Test Vector (201-250), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 201-250
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

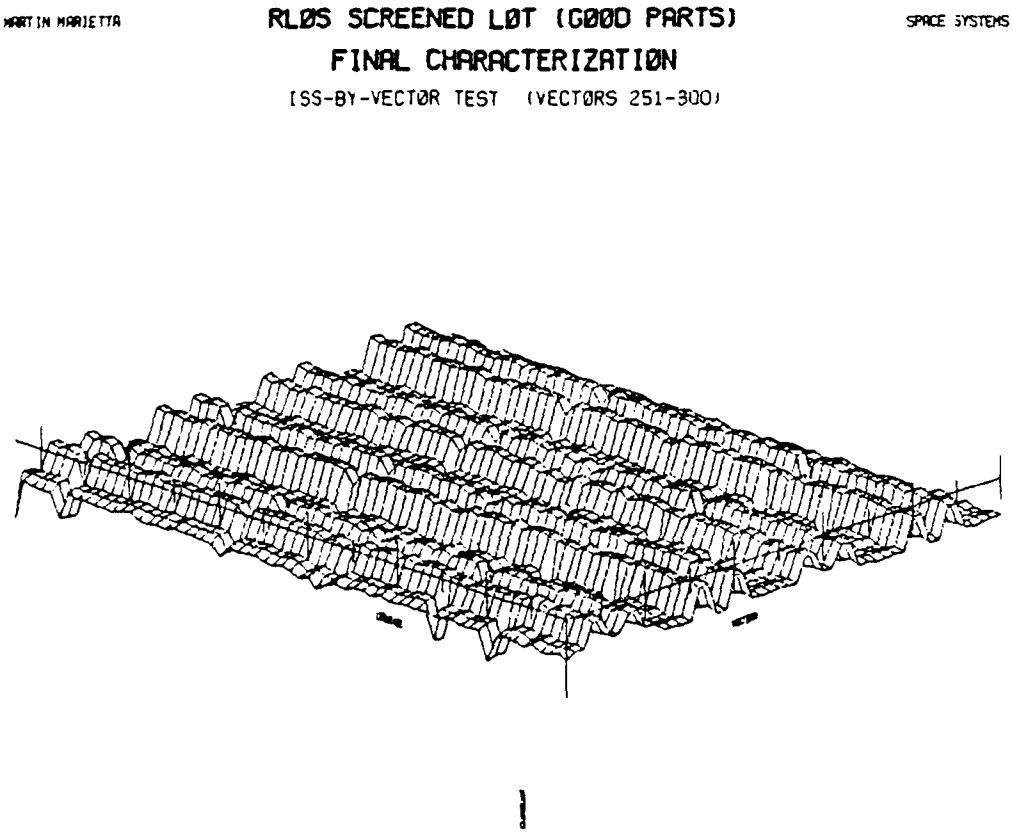

Figure 173 ISS vs Test Vector (251-300), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 251-300
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

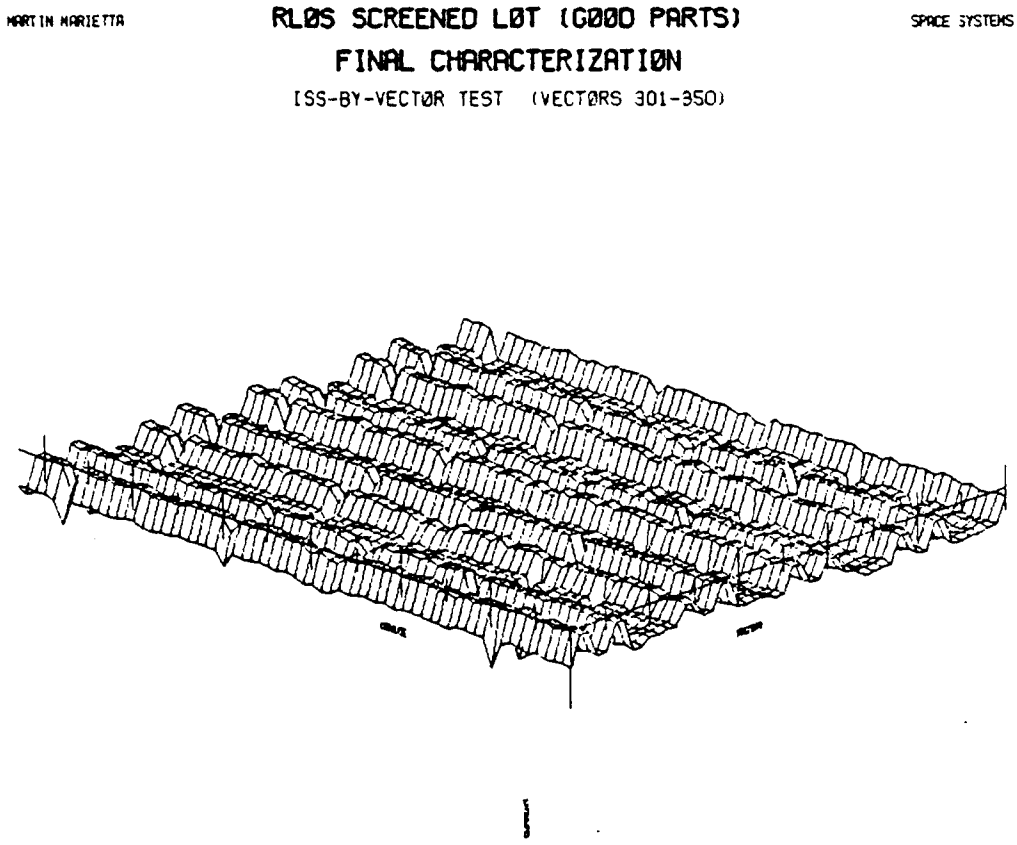

Figure 174 ISS vs Test Vector (301-350), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 301-350
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

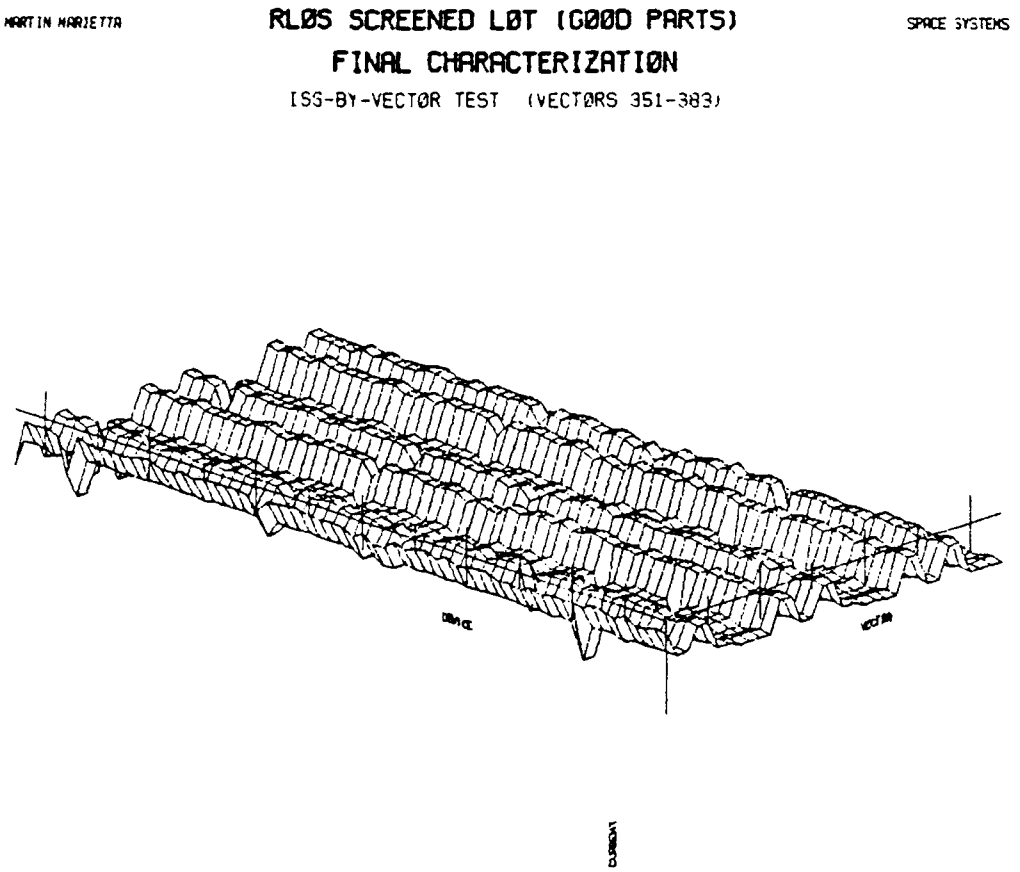

Figure 175 ISS vs Test Vector (351-383), Screened Lot, Final Data

Plot Information:

X-Axis: Vectors 351-383
Y-Axis: Devices 1-63
Z-Axis: ISS -10-0 mA

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